

PCN Number: CO-20896	Contact: Elizabeth La Greca				
Date Issued: July 23 <sup>rd</sup> , 2018	Title: Director, Sales Operations				
PCN Effective Date: November 23 <sup>rd</sup> , 2018	Phone: 1-858-795-0106				
Product(s) Affected: PE43704	Email: pcn@psemi.com				
Sample Availability: July 23 <sup>rd</sup> , 2018					
Change Control Board Approval #: CO-20896					
Change Category:					
	☐ Shipping/Labeling				
☐ Design/Mask Change	☐ Equipment				
☐ Singulation Process	☐ Material				
Assembly Process	☐ Product Specification				
☐ Electrical Test	☐ Product End of Life				
☐ Manufacturing Site	Other - Ordering codes change				
Purpose of Change:					
To enable Lapis as the primary wafer fabrication site	for the PE43704.				
Description of Change:					
MagnaChip closed their 150 mm wafer CMOS fab in South Korea at the end of 2015. To ensure there is no disruption to supply, we have been working to transfer products from MagnaChip fab to Lapis fab in Japan. Magnachip and Lapis are qualified Peregrine fabs.					
Lapis PE43704 material has been qualified with no change to form, fit, function or reliability. Please refer to the datasheet for the updated specs (PCN# CO-20889).					
Beginning <u>November 23<sup>rd</sup>, 2018</u> , the PE43704 shipped to customers will be supplied from either MagnaChip or Lapis wafers. Lapis will become the primary wafer fabrication site for the PE43704.					
Ordering code changes:					
Original ordering codes (MagnaChip): PE43704MLCA	-Z, EK43704-11				
New ordering codes (Lapis): PE43704B-Z, EK43704-	12				
pSemi manages inventory on a First-In First-Out (FIF change, please contact your account rep. or <u>account</u>					



Customer Acknowledgement of Receipt:

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☐ Change Denied	Name:	
(Include explanation in comments section below)	Title:	
☐ Change Approved	Company:	
	Date:	
	Signature:	
Customer Comments:		



### Appendix A – Reliability Qualification Summary



PE43704

### **Reliability Summary Report**

Part Number(s):	PE43704	Product Family:	DSA	
Package Type:	32L 5x5 QFN	MSL Rating:	MSL 1	
Technology Platform:	ULTRACMOS® 5			
Reliability Summary:		ation by similarity and the the reliability requiremen	results of reliability testing the ts for qualification.	

#### Table 1: Product Design Reliability Results

Test#	Test Performed	TEST METHOD/ Conditions	Duration	Req'd Sample Size <sup>2</sup> (#LOT x SS)	Actual Sample Size <sup>3</sup> (#LOT x SS)	Result (REJ/SS)
1	HTOL	JESD22-A108 VDD= 5.7V; Vss = -3.0V T <sub>A</sub> = T <sub>J</sub> = 150 °C;	500 Hrs.	1 x 77 devices	1 x 85 Devices	Passed (0/85)
2	ESD HBM	JS-001 / MIL-STD-883 Model 3015.7 (All pins)	1.5kV	1 x 3 devices	1 x 3 devices	Passed (0/3)
3	ESD MM	JEDEC JESD22-A115	200V	1 x 3 devices	1 x 3 devices	Passed (0/3)
4	ESD CDM	JEDEC JESD22-C101	250 V	1 x 3 devices	1 x 3 devices	Passed (0/3)





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# **Reliability Summary Report**

Table 2: Package Reliability Results

Test#	Test Performed	TEST METHOD/ Conditions	Duration	Req'd Sample Size <sup>2</sup> (#LOT x SS)	Actual Sample Size <sup>3</sup> (#LOT x SS)	Result (REJ/SS)
5	HTOL	JESD22-A108 VDD= 5.5 V; Vcntl= 3.6V; T <sub>A</sub> = T <sub>J</sub> = 150°C	500 hrs.	3 x 77 Devices	3 x 77 Devices	Passed (0/231)
6	HTS	JESD22-A103 T <sub>A</sub> = 150°C	1,000 hrs.	1 x 77 Devices	1 x 77 Devices	Passed (0/77)
7	HAST <sup>1</sup>	JESD22-A110 T <sub>A</sub> = 130°C; RH= 85%; VDD= 3.5 V; Vcntl= 3.5V	96 hrs.	3 x 45 Devices	3 x 45 Devices	Passed (0/135)
8	TC <sup>1</sup>	JESD22-A104 T <sub>A</sub> = -65°C to +150°C	500 cyc.	3 x 45 Devices	3 x 45 Devices	Passed (0/135)
9	TS <sup>1</sup>	JESD22—A105 T <sub>a</sub> = -55°C to +125°C	100 cyc.	3 x 45 devices	3 x 45 devices	Passed (0/135)





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### **Reliability Summary Report**

Table 3: Package Assembly Level Reliability Results

Test#	Test Performed	TEST METHOD/ Conditions	Duration	Req'd Sample Size <sup>2</sup> (#LOT x	Actual Sample Size <sup>3</sup> (#LOT x	Result (REJ/SS)
10	WBP	JESD22-B115/ Subcon specs.	-	3 x 171 Wires	3 x 171 Wires	Passed (0/513)
11	Physical Dimensions	JESD22-B100	-	3 x 10 Devices	3 x 10 Devices	Passed (0/30)
12	Die Shear	Mil-Std-883 M2019.8	-	3 x 3 Devices	3 x 3 Devices	Passed (0/9)
13	Solderability	JESD22-B102	-	3 x 12 Devices	3 x 12 Devices	Passed (0/36)





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# **Reliability Summary Report**

Table 4: Wafer Process Reliability Results

Test#	Test Performed	TEST METHOD/ Conditions	Duration	Req'd Sample Size <sup>2</sup> (#LOT x SS)	Actual Sample Size <sup>3</sup> (#LOT x SS)	Result (REJ/SS)
14	HTOL	JESD22-A108 VDD= 4.8V; VCTL = 1.8V T <sub>A</sub> = T <sub>J</sub> = 150 °C;	500 hrs.	3 x 77 Devices	3 x 77 Devices	Passed (0/231)
15	HTS	JESD22-A103 T <sub>a</sub> = 150°C	1,000 hrs.	1 x 77 Devices	3 x 77 Devices	Passed (0/231)
16	HAST <sup>1</sup>	JESD22-A110 T <sub>a</sub> = 130°C; RH= 85%; P <sub>v</sub> = 2.27 atm; biased	234 hrs.	3 x 45 Devices	3 x 45 Devices	Passed (0/135)
17	TC <sup>1</sup>	JESD22-A104 T <sub>a</sub> = -55°C to +125°C	500 cyc.	3 x 45 Devices	3 x 45 Devices	Passed (0/135)
18	Electro- migration <sup>4</sup>	JESD61A / Foundry Spec	>T50	1 x 1 wafer	1 x 1 wafer	Passed (0/1)
19	Passivation Integrity <sup>4</sup>	Internal Specification DOC -00373 / Foundry Spec	-	1 x 1 wafer	1 x 1 wafer	Passed (0/1)
20	Destructive / Construction Analysis <sup>4</sup>	Internal Specification DOC -00373 / Foundry Spec	N/A	1 x 1 wafer	1 x 1 wafer	Passed (0/1)
21	Hot Carrier <sup>4</sup>	JESD28 / JESD60A Foundry Spec	>T50	1 x 1 wafer	1 x 2 wafer	<u>Passed</u> (0/2)
22	TDDB⁴	JESD92 / Foundry Spec	>T50	3 x 2 wafer	3 x 2 wafer	Passed (0/6)

<sup>&</sup>lt;sup>1</sup> J-STD-020, Level-1 pre-conditioning applied: Moisture Soak at 85°C/85% RH for 168 hours. Reflow at 260±0.5°C.

<sup>&</sup>lt;sup>2</sup> Required sample size is based on Peregrine Semiconductor's internal Reliability qualification requirements.

<sup>3</sup> Actual sample size may be more than the required sample size to maximize the use of Reliability hardware.

<sup>&</sup>lt;sup>4</sup> Actual sample size may be more depending on different Transistor type, structure, and stress conditions used as per PSC Internal spec