Considerations Using PE29100 EVB with EPC8009 eGaN FETs

Application Note 64

Summary

The PE29100 evaluation board (EVB) populated with EPC8009 enhancement mode power transistors allows the user to evaluate the PE29100 high-speed driver in a half-bridge configuration. The following topics are intended to point out general guidelines when designing with the high-speed driver.

- Bootstrap overcharging
- Minimum pulse width
- False triggering effect caused by negative inductor current
- Maximum input operating voltage
- Operating frequency range

Introduction

The PE29100 integrated high-speed driver is designed to control the gates of external power devices such as enhancement mode gallium nitride (eGaN®) field effect transistors (FETs). The outputs of the PE29100 are capable of providing switching transition speeds in the sub nanosecond range for hard switching applications up to 33 MHz.

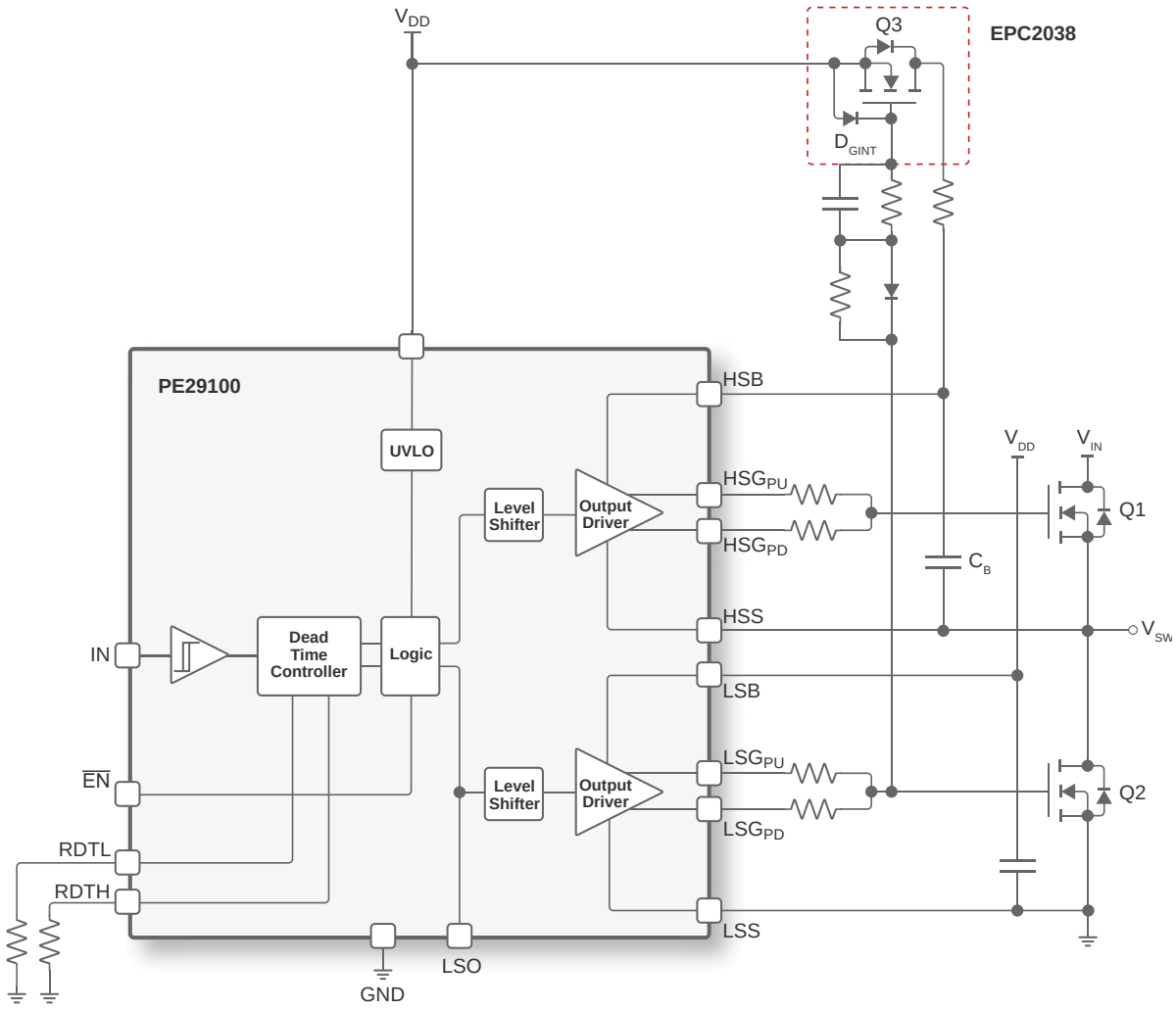
Certain precautions need to be observed when designing with the PE29100 driver. This document identifies the operational limits of the PE29100 in a half-bridge configuration using two EPC8009 eGaN FETs. Operating the circuit beyond these recommended limits can result in damage to both the driver and power transistors.

Bootstrap Overcharging

Bootstrap overcharging is an artifact of the half-bridge topology when using a high-side bootstrap diode. When a large voltage drop across the low-side FET conducts current through it's body diode during the dead-time period after the low-side device turns off and before the high-side device turns on, an overvoltage condition across the bootstrap capacitor can result. This could potentially damage the high-side device by exceeding its gate-to-source voltage specification. Placing a small external resistor in series with the high-side bootstrap diode can limit the charging speed of the bootstrap capacitor to prevent overvoltage. However, this approach becomes condition dependent as the load current and/or dead-time range increases.

A more elegant approach replaces the high-side bootstrap diode with an eGaN FET (**Figure 1**). The EPC2038 is used as a synchronous bootstrap FET to prevent overvoltage of the upper device. The eGaN FET includes an internal diode and has a large forward drop that can limit the overvoltage, but all of the charging must occur during the dead-time. This is accomplished through synchronous switching with the low-side device if a body diode voltage drop occurs.

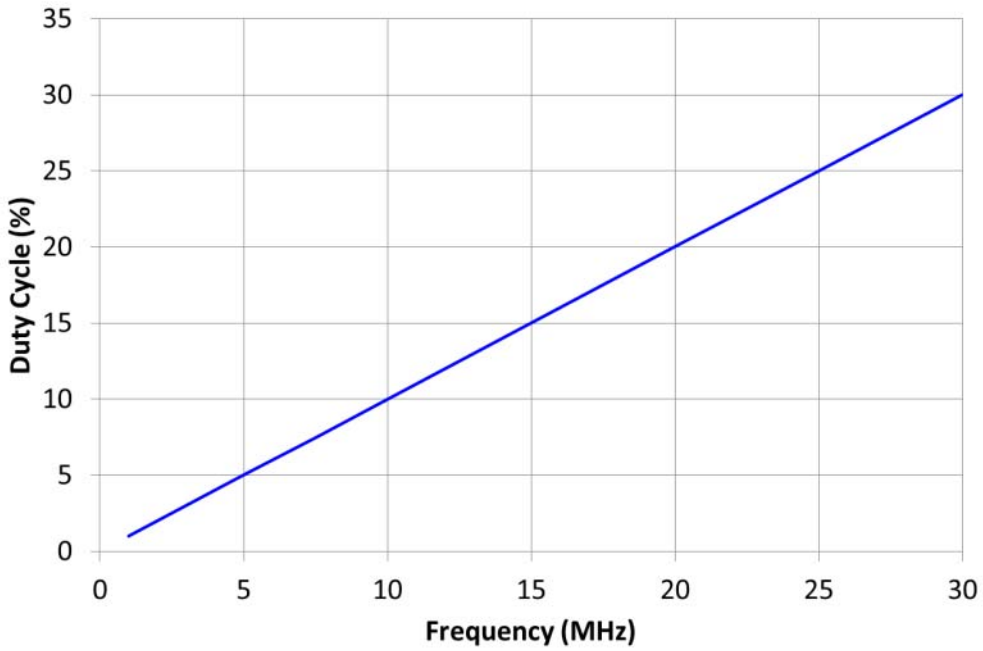
Figure 1 • *PE29100 Applications Schematic Showing Synchronous Bootstrap FET*



Minimum Pulse Width

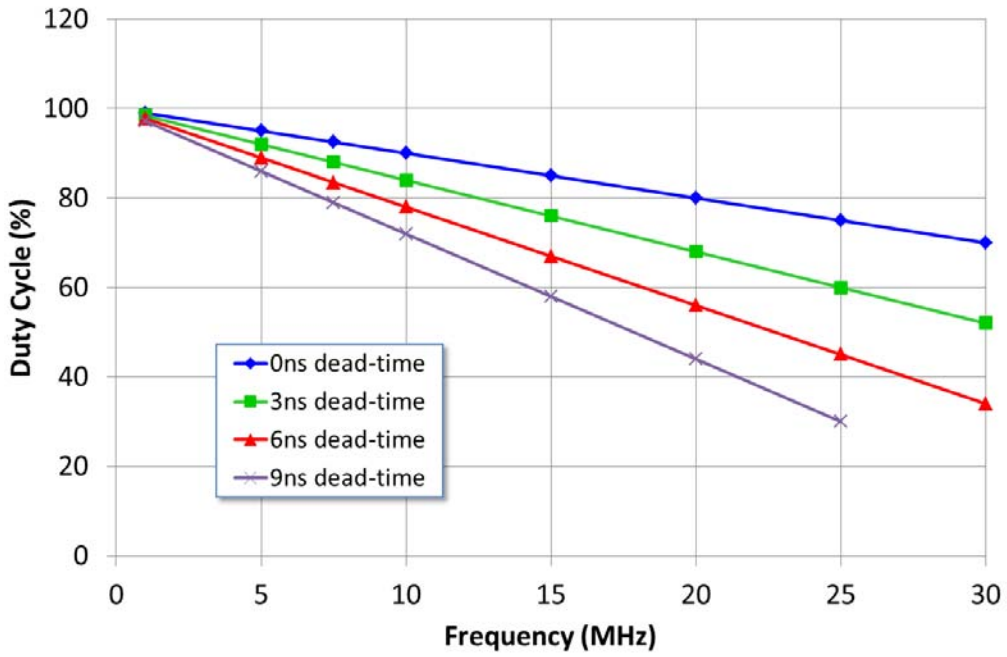
The minimum positive output pulse width should be limited to 10 ns. Operating the positive pulse width below 10 ns can result in a steady ON state condition to the high-side gate; therefore, potentially damaging the high-side device. A similar condition can result to the low-side output if the minimum negative pulse width extends below 10 ns. The low-side output is an inverse of the input signal and its pulse width depends on the dead-time value. Figure 2 and Figure 3 show the relationship between operating frequency and duty cycle for the high-side and low-side minimum output pulse width for different dead-time settings. For example, a minimum negative pulse width of 10 ns at 5 MHz will result in a maximum duty cycle of 95%, but at 25 MHz it is only a 75% maximum duty cycle with no dead-time.

Figure 2 • *Duty Cycle Limit for 10 ns High-side Output Pulse Independent of Dead-time Setting*



Note: * Area above line safe.

Figure 3 • *Duty Cycle Limit for 10 ns Low-side Output Pulse Width*



Note: * Area below line safe.

False Triggering Effect Caused by Negative Inductor Current

The false triggering effect is a function of the chip design where the level shifter timing pulse is superseded by a negative inductor current flow through the low-side device causing a false timing trigger and forcing the high-side driver to drop-out. During this low-to-high switching transition, the dead-time should be limited to 4 ns when a negative current is flowing from source to drain. Above 4 ns and under no load conditions, reverse current can result in cycle skipping of the HSG. For applications requiring dead-time ranges beyond 4 ns and in the presence of reverse inductor current, the dv/dt of SW node should be less than 2.5V per nanosecond.

Maximum Input Operating Voltage

The maximum operating voltage should be limited to 30V when driving the EPC8009 eGaN FETs in a half-bridge configuration. Exceeding 30V can result in damage due to high dv/dt sensitivity on the HSS pin.

Operating Frequency Range

The switching frequency should be limited to 5 MHz–33 MHz. There is an LC connected to the half-bridge in order to generate an output voltage (V_{OUT}). The value of the inductor is 0.12 uH. The minimum operating frequency should be limited to 5 MHz due to excessive input current ripple that can potentially damage the eGaN FETs.The ripple on the inductor needs to be kept at 30% of maximum load current (2A) and make sure the peak inductor current does not reach the maximum rating of the eGaN FETs. The frequency and duty cycle adjustments must be done to maintain the safe operating area of the EVK components. There is no over current protection or overvoltage protection provided on this EVB.

Conclusion

This document is intended to address operating limits that have been observed on the PE29100 evaluation board driving EPC8009 eGaN FETs in a half-bridge configuration. Operating the circuit beyond these recommended limits can result in damage to both the driver and power transistors.

Sales Contact

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