

PE42422

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 5–6000 MHz



Features

- Symmetric SPDT reflective switch
- Low insertion loss:
 - 0.23 dB typical @ 100 MHz
 - 0.25 dB typical @ 1000 MHz
 - 0.40 dB typical @ 3000 MHz
 - 0.65 dB typical @ 5000 MHz
 - 0.90 dB typical @ 6000 MHz
- Wide supply range: 2.3–5.5V
- Excellent linearity:
 - IIP2 of 105 dBm @ 17 MHz
 - IIP3 of 81 dBm @ 17 MHz
- High ESD tolerance:
 - 4 kV HBM on RF pins to GND
 - 1 kV on all other pins
- Logic Select (LS) pin provides maximum flexibility of control logic

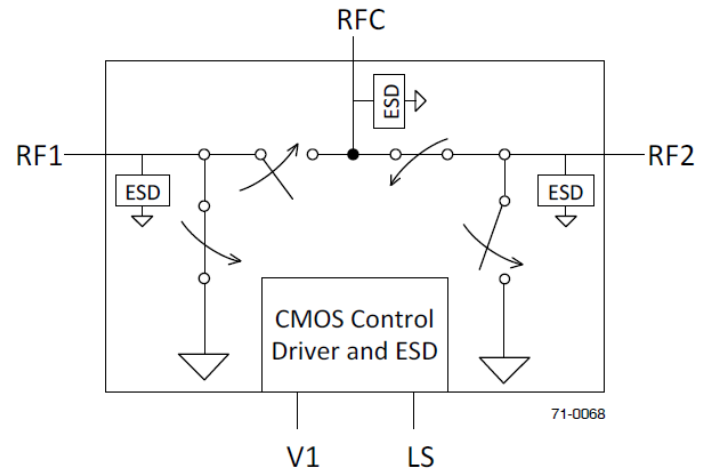



Figure 1. PE42422 functional block diagram

Product description


The PE42422 is a HaRP™ technology-enhanced SPDT RF switch designed to cover a broad range of applications from 5–6000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface and requires no external components.

pSemi's HaRP technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

 Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

 When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42422 absolute maximum ratings

Parameter or condition	Min	Max	Unit
RF input power, 50Ω ⁽¹⁾ : 5–100 MHz 100–6000 MHz	–	33 34	dBm dBm
ESD voltage HBM ⁽²⁾ : RF pins to GND All other pins	–	4000 1000	V V
ESD voltage MM, all pins ⁽³⁾	–	200	V
Storage temperature (T _{ST})	–65	+150	°C



1. V_{DD} within the operating range specified in [Table 2](#).
2. Human Body Model (MIL_STD 883 Method 3015.7).
3. Machine Model (JEDEC JESD22-A115-A).

Recommended operating conditions

Table 2 lists the PE42422 recommending operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42422 operating conditions

Parameter	Min	Typ	Max	Unit
VDD supply voltage	2.3	3.3	5.5	V
IDD power supply current	–	120	200	μA
RFx–RFc input power	–	–	See Figure 2 .	dBm
Control voltage high	1.2	1.5	3.3	V
Control voltage low	0	0	0.5	V
Operating temperature range	–40	+25	+85	°C


Electrical specifications

Table 3 lists the PE42422 key electrical specifications at +25 °C⁽¹⁾, V_{DD} = 2.3–5.5V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42422 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency	–	–	5	–	6000	MHz
Insertion loss ⁽²⁾	RFx–RFc	5–100 MHz	–	0.23	–	dB
		100–1000 MHz	–	0.25	0.35	dB
		1000–2000 MHz	–	0.30	0.40	dB
		2000–3000 MHz	–	0.40	0.50	dB
		3000–4000 MHz	–	0.50	0.70	dB
		4000–5000 MHz	–	0.65	0.90 ⁽²⁾	dB
		5000–6000 MHz	–	0.90	1.25 ⁽²⁾	dB
Isolation	RFx–RFc	5–100 MHz	–	68	–	dB
		100–1000 MHz	42	44	–	dB
		1000–2000 MHz	33	35	–	dB
		2000–3000 MHz	27	29	–	dB
		3000–4000 MHz	22	24	–	dB
		4000–5000 MHz	18	20	–	dB
		5000–6000 MHz	15	17	–	dB
Isolation	RFx–RFx	5–100 MHz	–	61	–	dB
		100–1000 MHz	40	41	–	dB
		1000–2000 MHz	32	33	–	dB
		2000–3000 MHz	26	28	–	dB
		3000–4000 MHz	22	24	–	dB
		4000–5000 MHz	18	20	–	dB
		5000–6000 MHz	15	16	–	dB
Return loss ⁽²⁾	RFx–RFc	5–100 MHz	–	33	–	dB
		100–1000 MHz	–	28	–	dB
		1000–2000 MHz	–	21	–	dB
		2000–3000 MHz	–	20	–	dB

Parameter	Path	Condition	Min	Typ	Max	Unit
		3000–4000 MHz	–	18	–	dB
		4000–5000 MHz	–	16 ⁽²⁾	–	dB
		5000–6000 MHz	–	13 ⁽²⁾	–	dB
Second harmonic	RFx–RFc	+18 dBm input power, 17–204 MHz	–	-92	–	dBc
		+32 dBm output power, 850/900 MHz	–	-99	–	dBc
		+32 dBm output power, 1800/1900 MHz	–	-101	–	dBc
Third harmonic	RFx–RFc	+18 dBm input power, 17–204 MHz	–	-125	–	dBc
		+32 dBm output power, 850/900 MHz	–	-93	–	dBc
		+32 dBm output power, 1800/1900 MHz	–	-87	–	dBc
IMD3	RFx–RFc	Bands I, II, V, VIII +17 dBm CW @ TX freq at RFC, –15 dBm CW @ 2Tx-Rx at RFC, 50Ω	–	-115	–	dBm
IIP2	RFx	5 MHz	–	96	–	dBm
		17 MHz	–	105	–	dBm
		100–6000 MHz	–	115	–	dBm
IIP3	RFx	5 MHz	–	75	–	dBm
		17 MHz	–	81	–	dBm
		100–6000 MHz	–	75	–	dBm
Input 0.1dB compression point ⁽³⁾	RFx or RFc	5–100 MHz	–	33	–	dBm
		100–6000 MHz	–	34	–	dBm
Switching time	–	50% CTRL to (10%–90%) or (90%–10%) RF	–	2	4	μs

-  1. Typical performance over temperature and V_{DD} as shown in [Figure 3](#) through Figure 19.
2. You can improve high frequency performance with external matching. For details, see [Figure 20](#) through Figure 25 and [Figure 28](#).
3. The input P0.1dB compression point is a linearity figure of merit. For the operating RF input power, see [Table 2](#).

SPDT control logic

Table 4. PE42422 truth table.

Path	V1	LS
RFc–RF2	1	1
RFc–RF1	0	1
RFc–RF1	1	0
RFc–RF2	0	0

Power de-rating curve

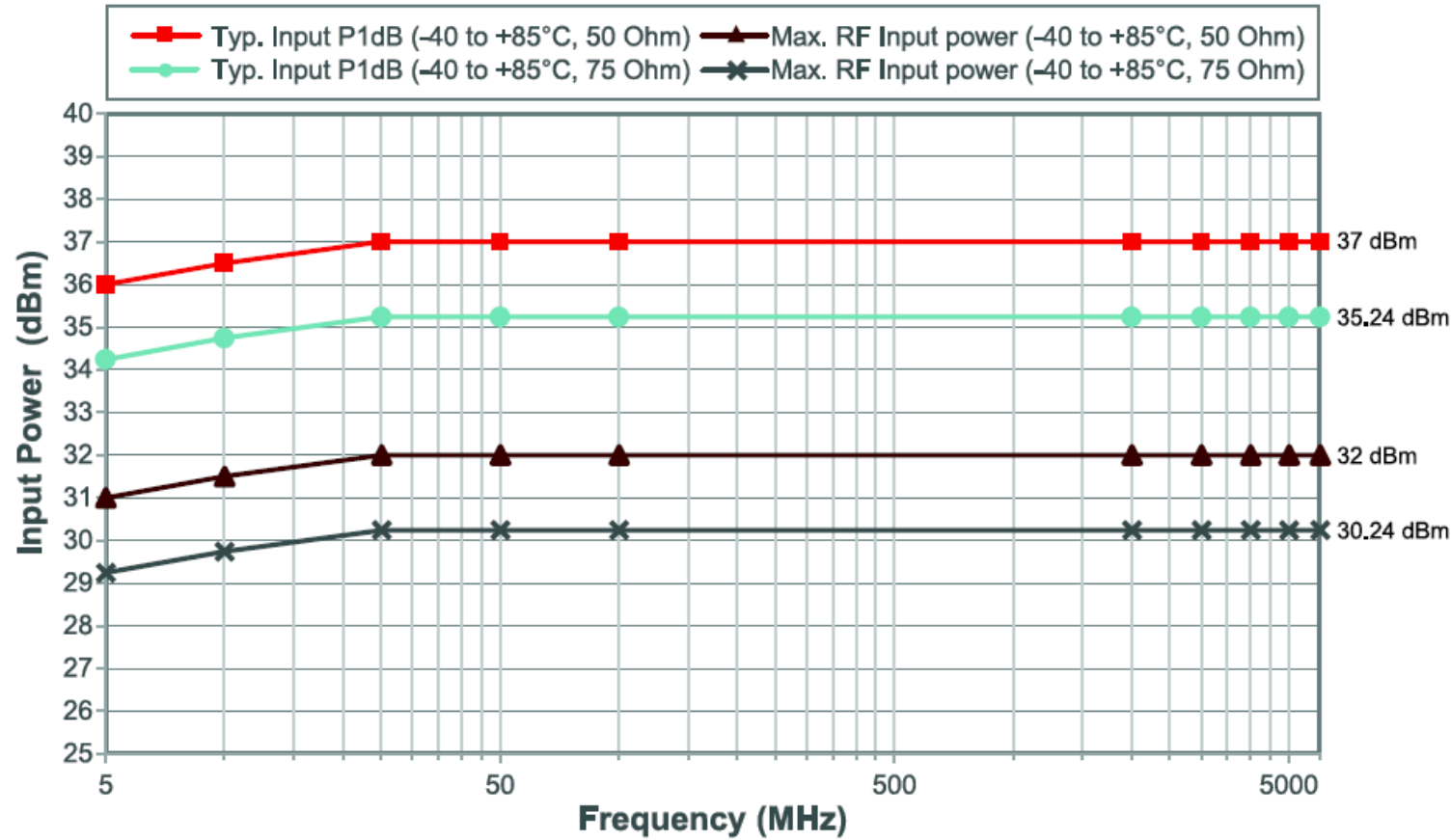


Figure 2. Power de-rating curve for 5–6000 MHz

Typical performance data

Figure 3–Figure 19 show the typical performance data at +25 °C and $V_{DD} = 3.3V$, unless otherwise specified.

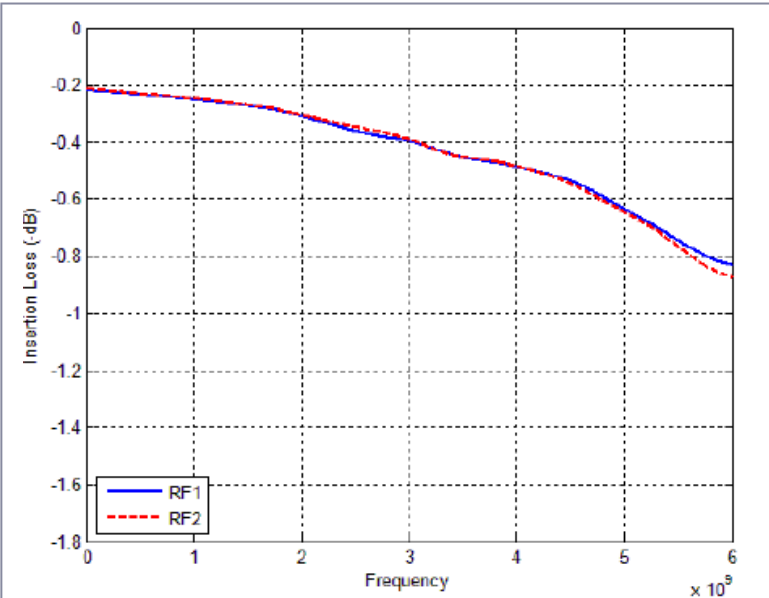


Figure 3. Insertion loss RFx(*)

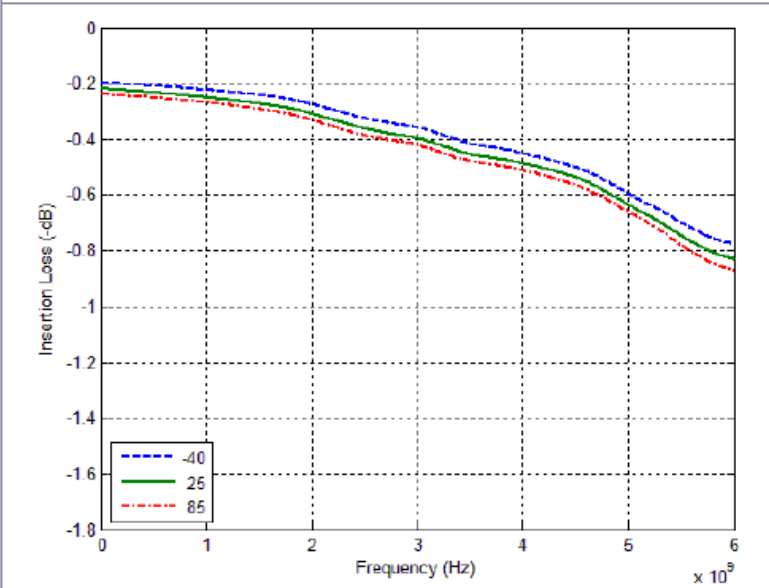


Figure 4. Insertion loss vs. temperature (RF1–RFc)(*)

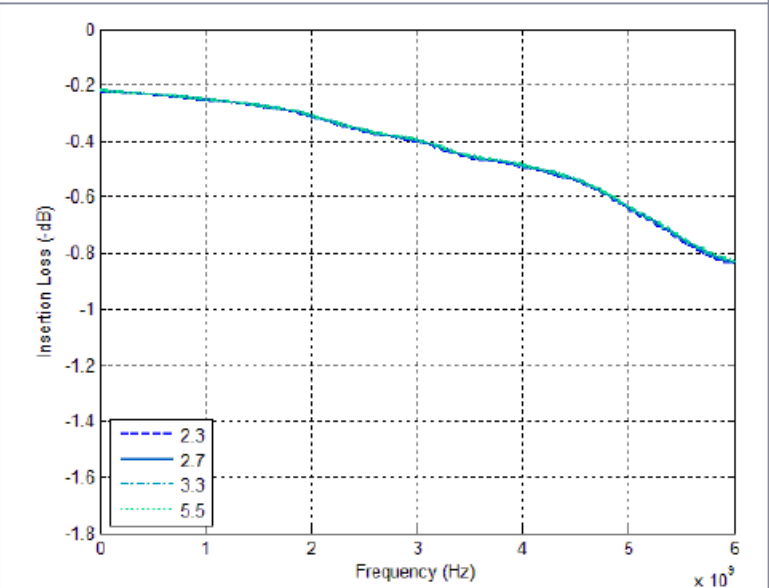


Figure 5. Insertion loss vs. VDD (RF1–RFc)(*)

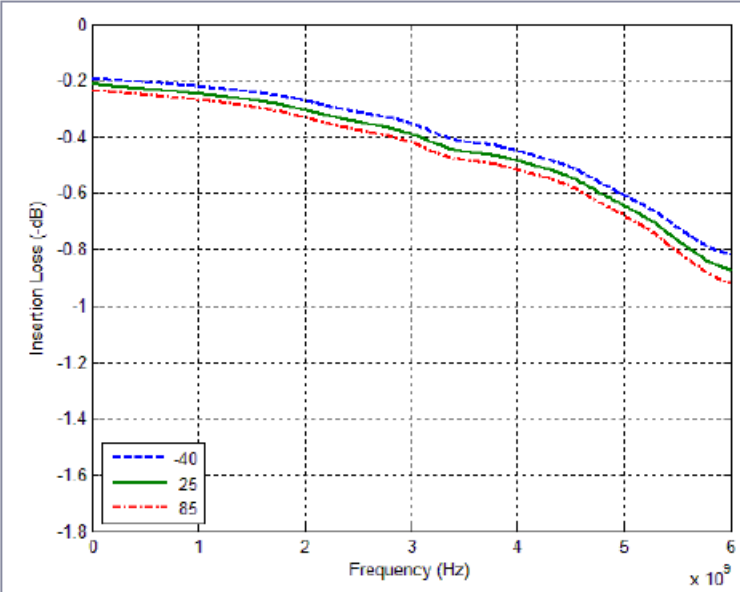


Figure 6. Insertion loss vs. temperature (RF2-RFc)(*)

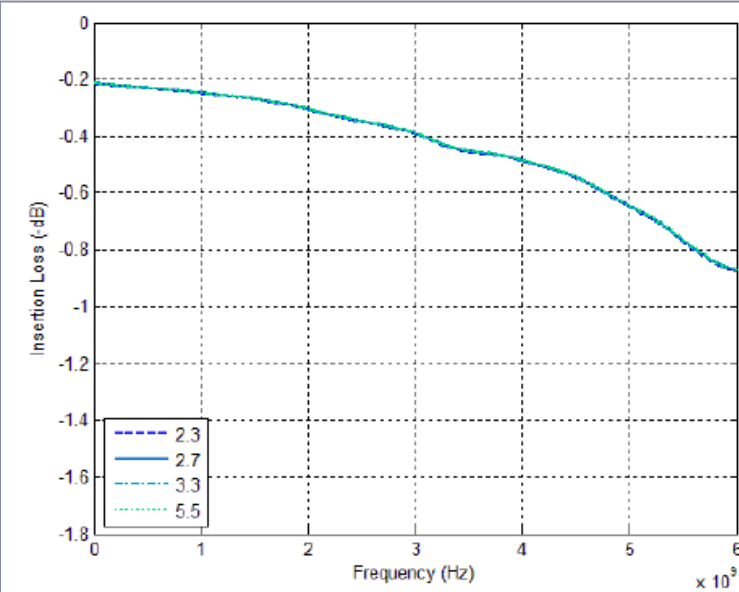


Figure 7. Insertion loss vs. VDD (RF2-RFc)(*)

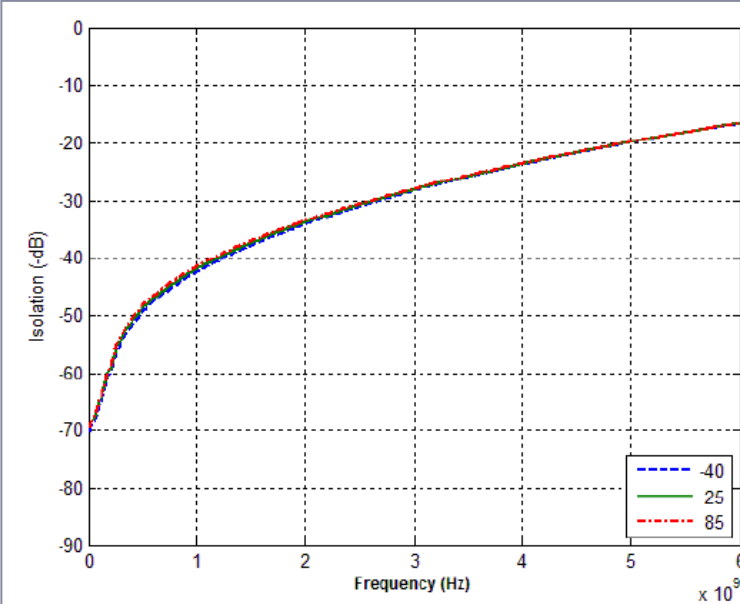


Figure 8. RFx-RFx isolation vs. temperature

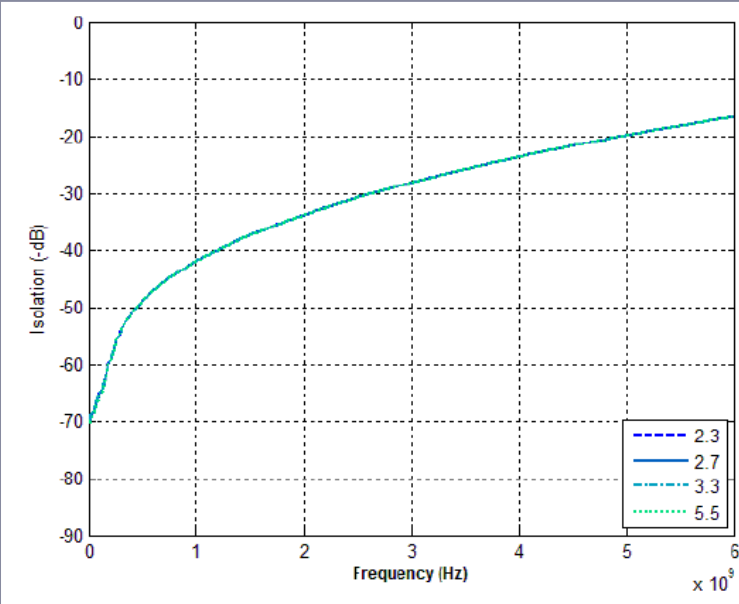


Figure 9. RFx-RFx isolation vs. VDD

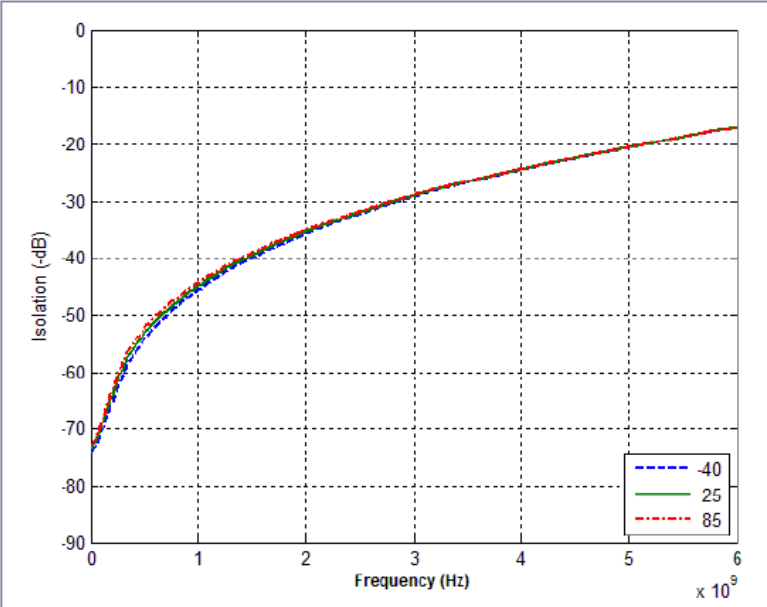


Figure 10. RFc-RFx isolation vs. temperature

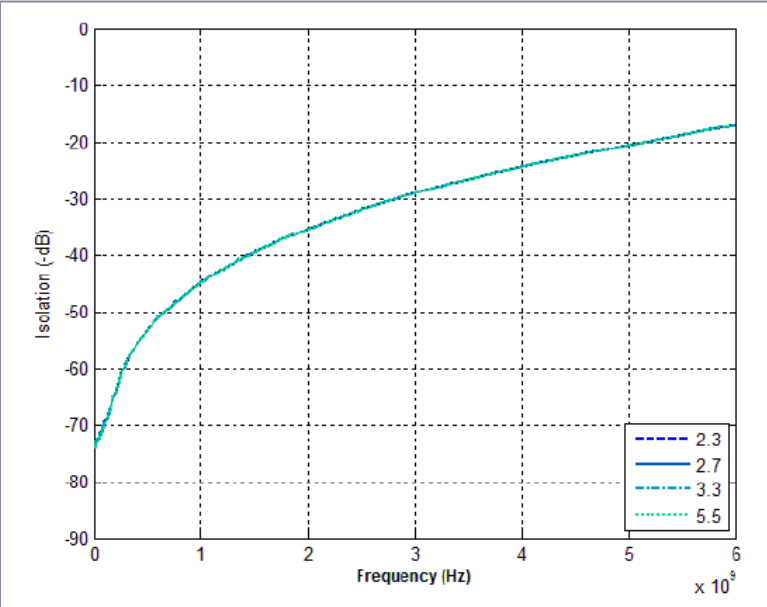


Figure 11. RFc-RFx isolation vs. VDD

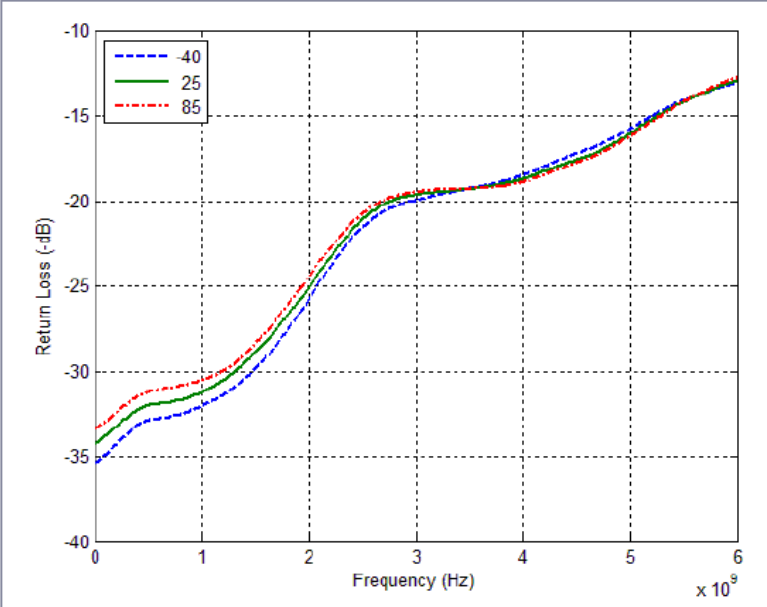


Figure 12. RFc port return loss vs. temperature (RF1 active)(*)

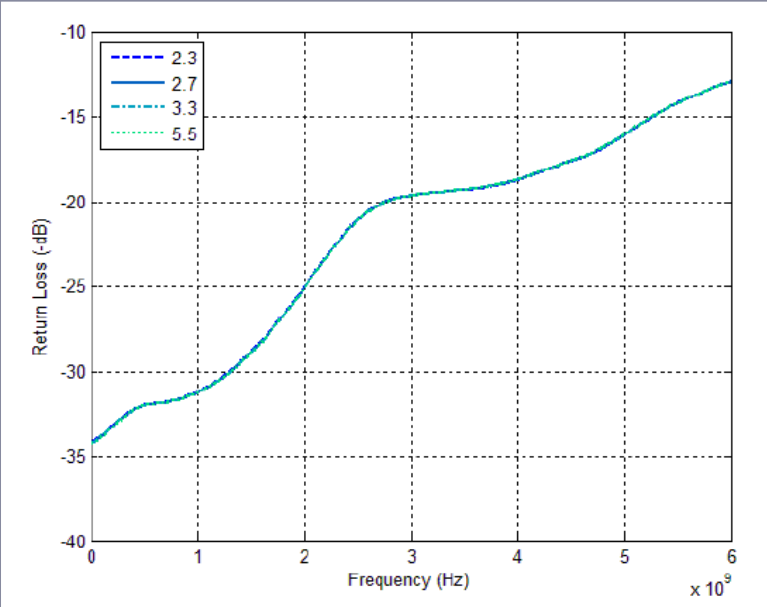


Figure 13. RFc port return loss vs. VDD (RF1 active)(*)

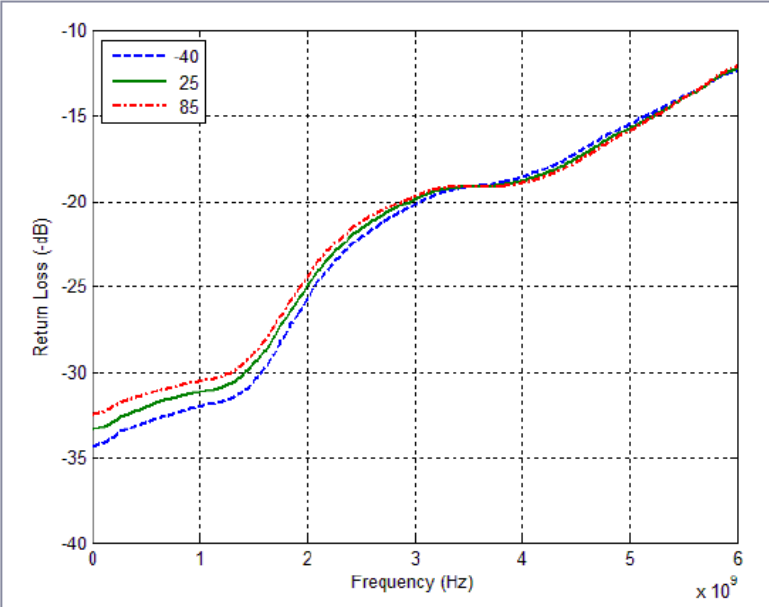


Figure 14. RFc port return loss vs. temperature (RF2 active)(*)

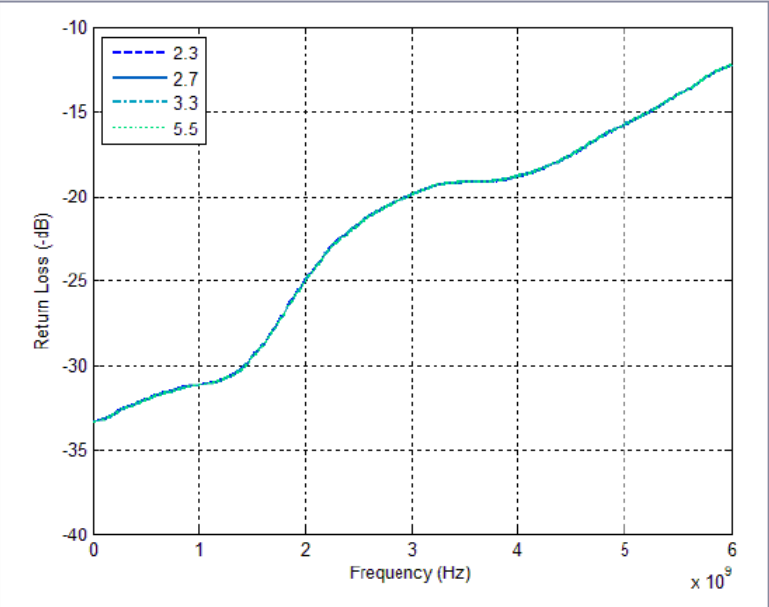


Figure 15. RFc port return loss vs. VDD (RF2 active)(*)

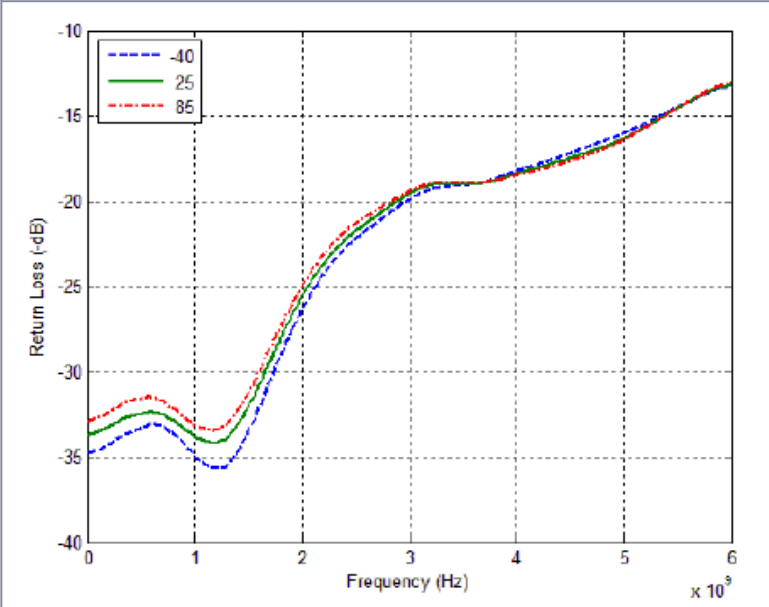


Figure 16. Active port return loss vs. temperature (RF1 active)(*)

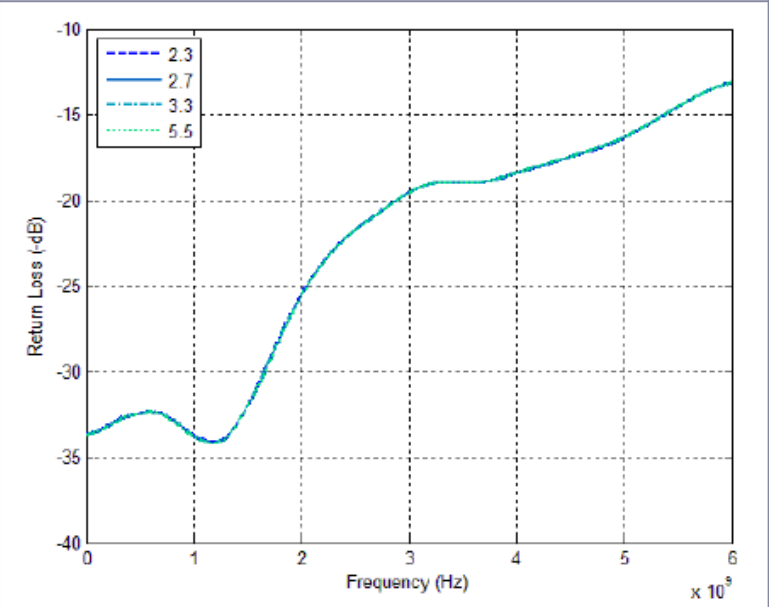
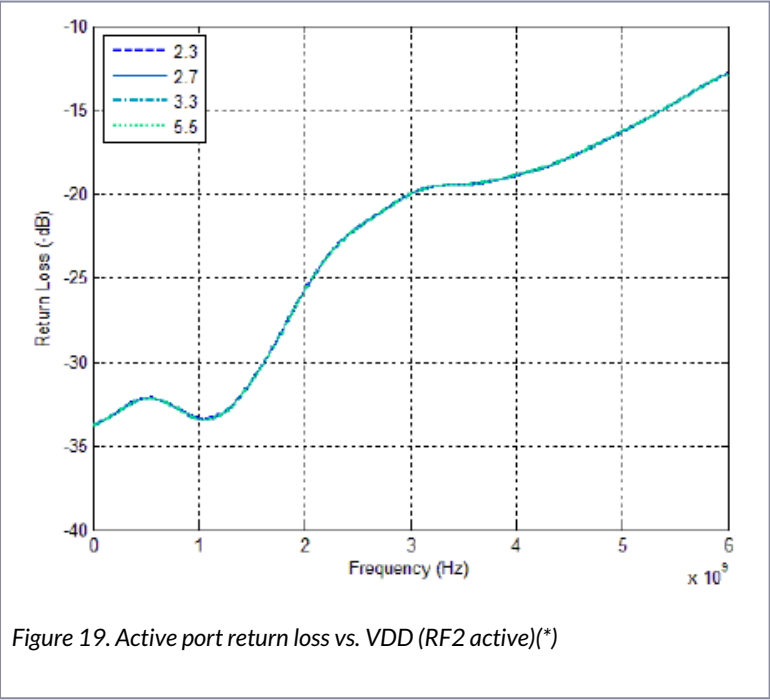
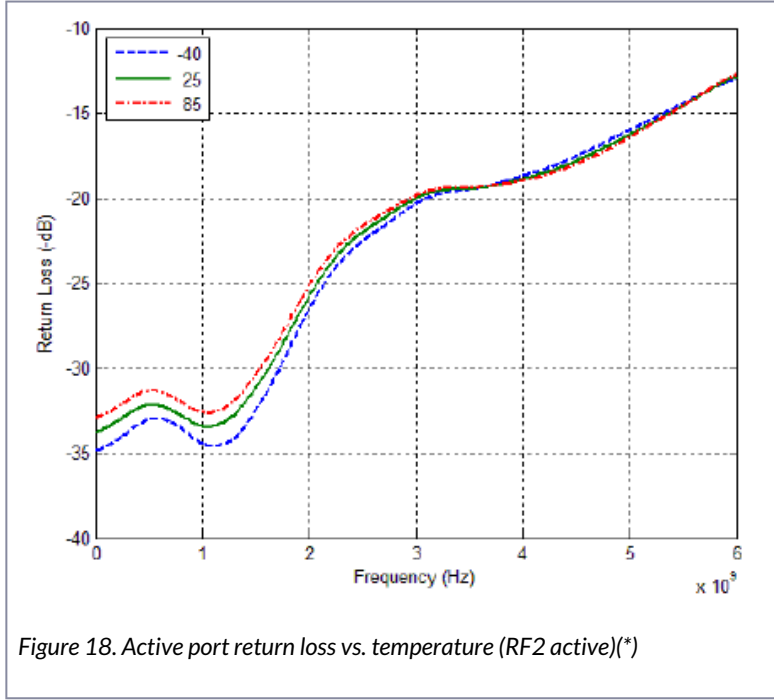


Figure 17. Active port return loss vs. VDD (RF1 active)(*)



i * You can improve high frequency performance with external matching. For details, see [Figure 20](#) through [Figure 25](#) and [Figure 28](#).

Figure 20–Figure 25 show the performance comparison data at +25 °C and $V_{DD} = 3.3V$, with and without matching.

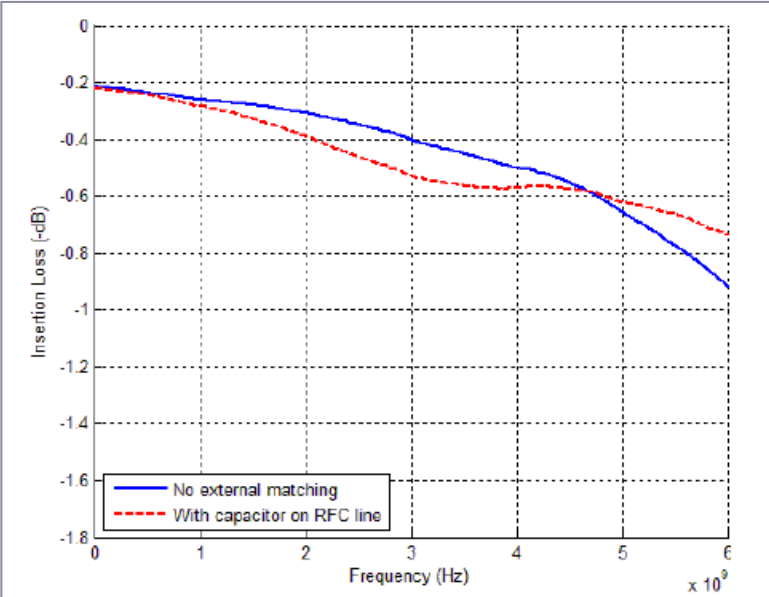


Figure 20. Insertion loss RF1(*)

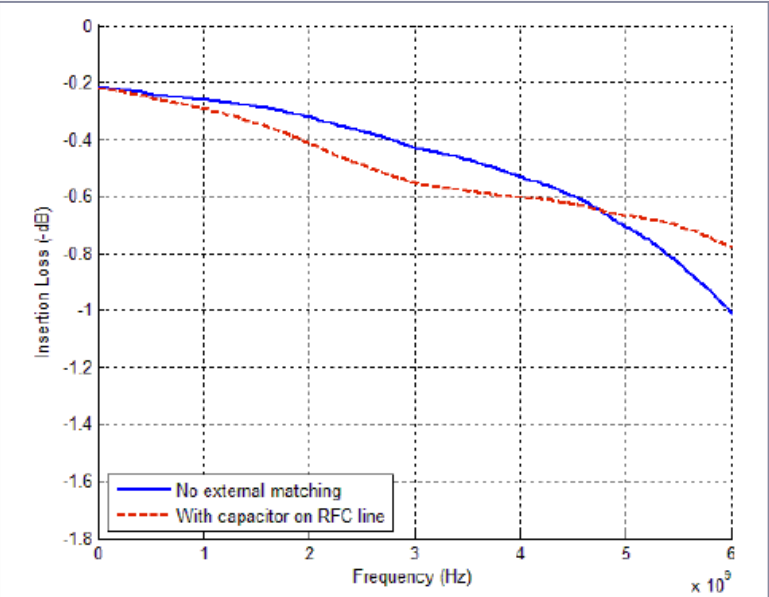


Figure 21. Insertion loss RF2(*)

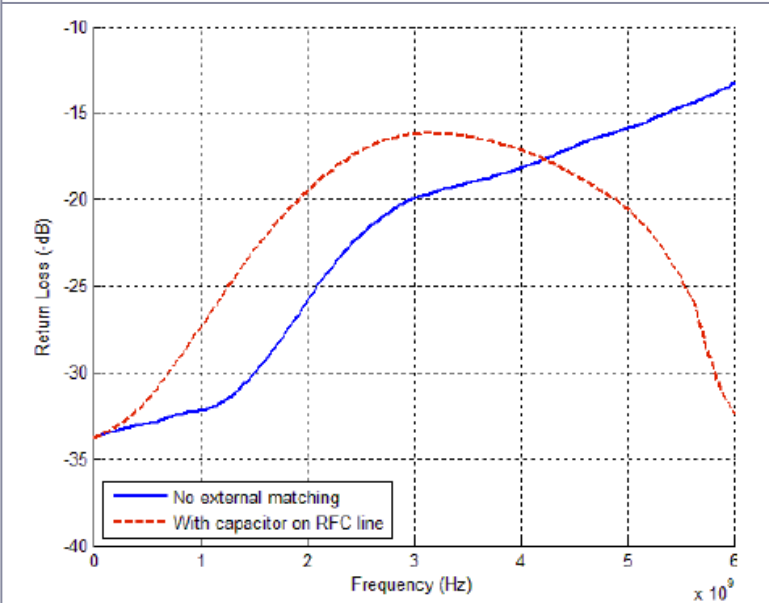


Figure 22. Active port return loss (RF1 active)(*)

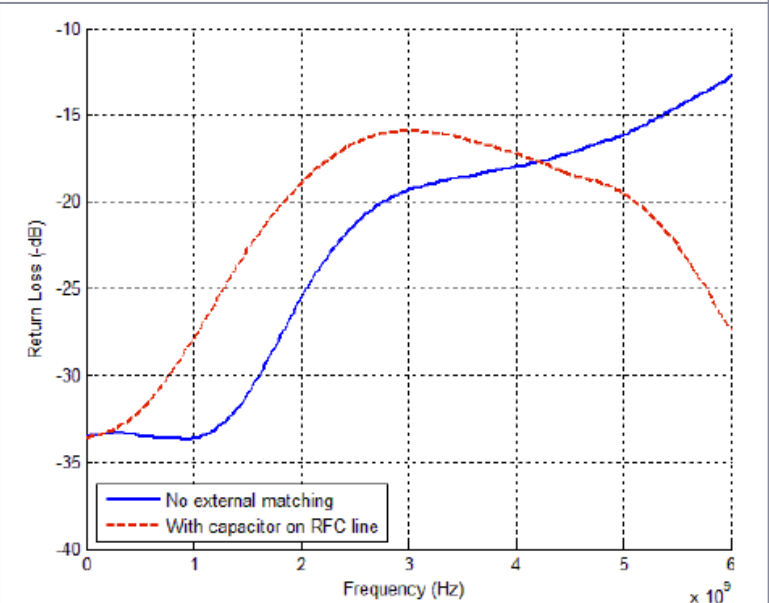


Figure 23. Active port return loss (RF2 active)(*)

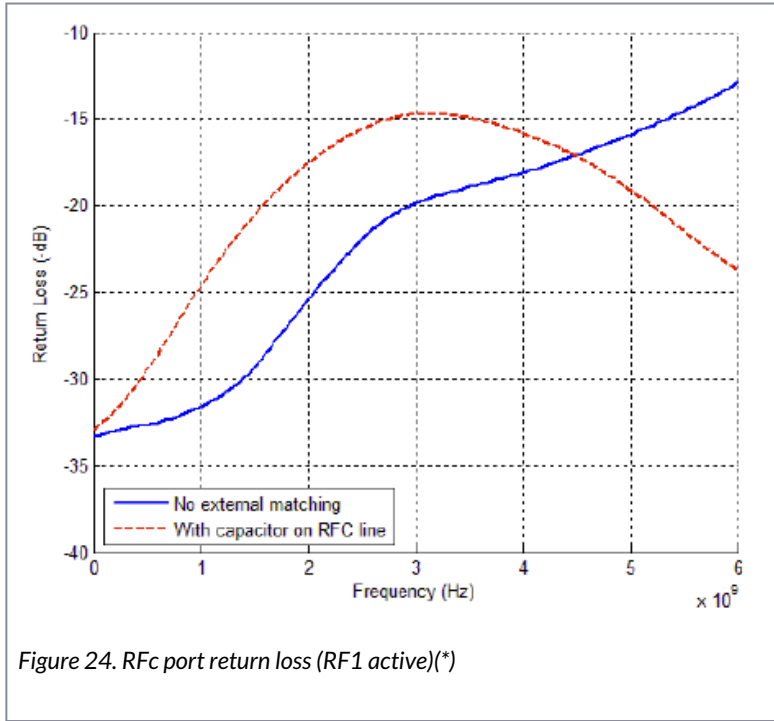


Figure 24. RFc port return loss (RF1 active)(*)

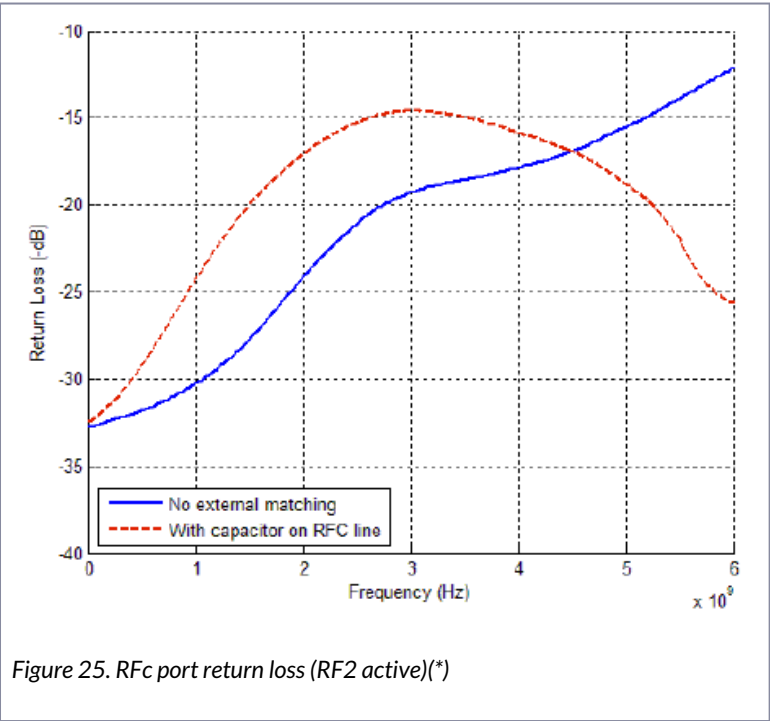


Figure 25. RFc port return loss (RF2 active)(*)



- You can improve high frequency performance with external matching. For details, see [Figure 20](#) through [Figure 25](#) and [Figure 28](#).

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the PE42422. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J2. The RF1 and RF2 ports connect through 50Ω transmission lines via SMA connectors J1 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. J8 provides DC and digital inputs to the device.

The board is constructed of a four-layer metal material with a total thickness of 62 mils. The top and bottom RF layers are Rogers RO4350 material with a 10-mil RF core. The middle layers provide ground for the transmission lines. pSemi designed the transmission lines using a coplanar waveguide with a ground plane model using a trace width of 22 mils, trace gaps of 7 mils, and a metal thickness of 2.1 mils.

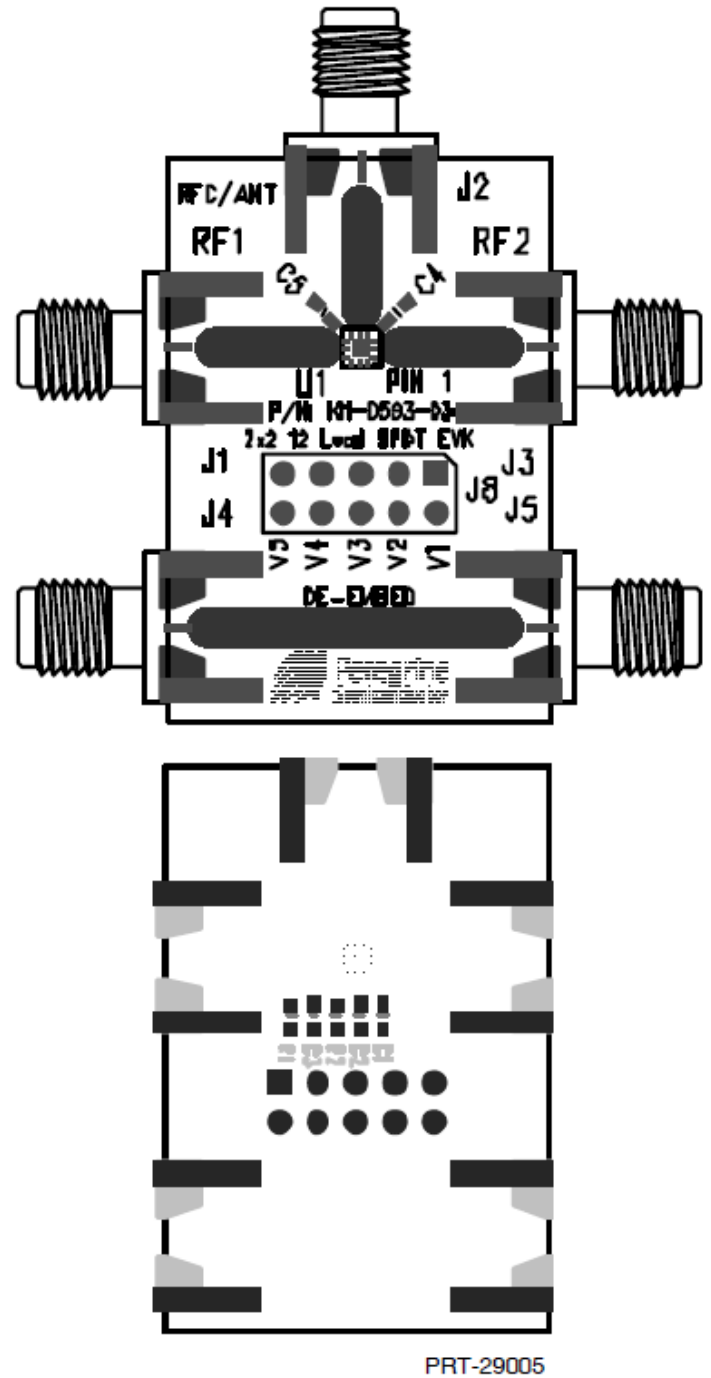


Figure 26. Evaluation board layout

Evaluation board schematics

Figure 27 shows the evaluation board schematic.

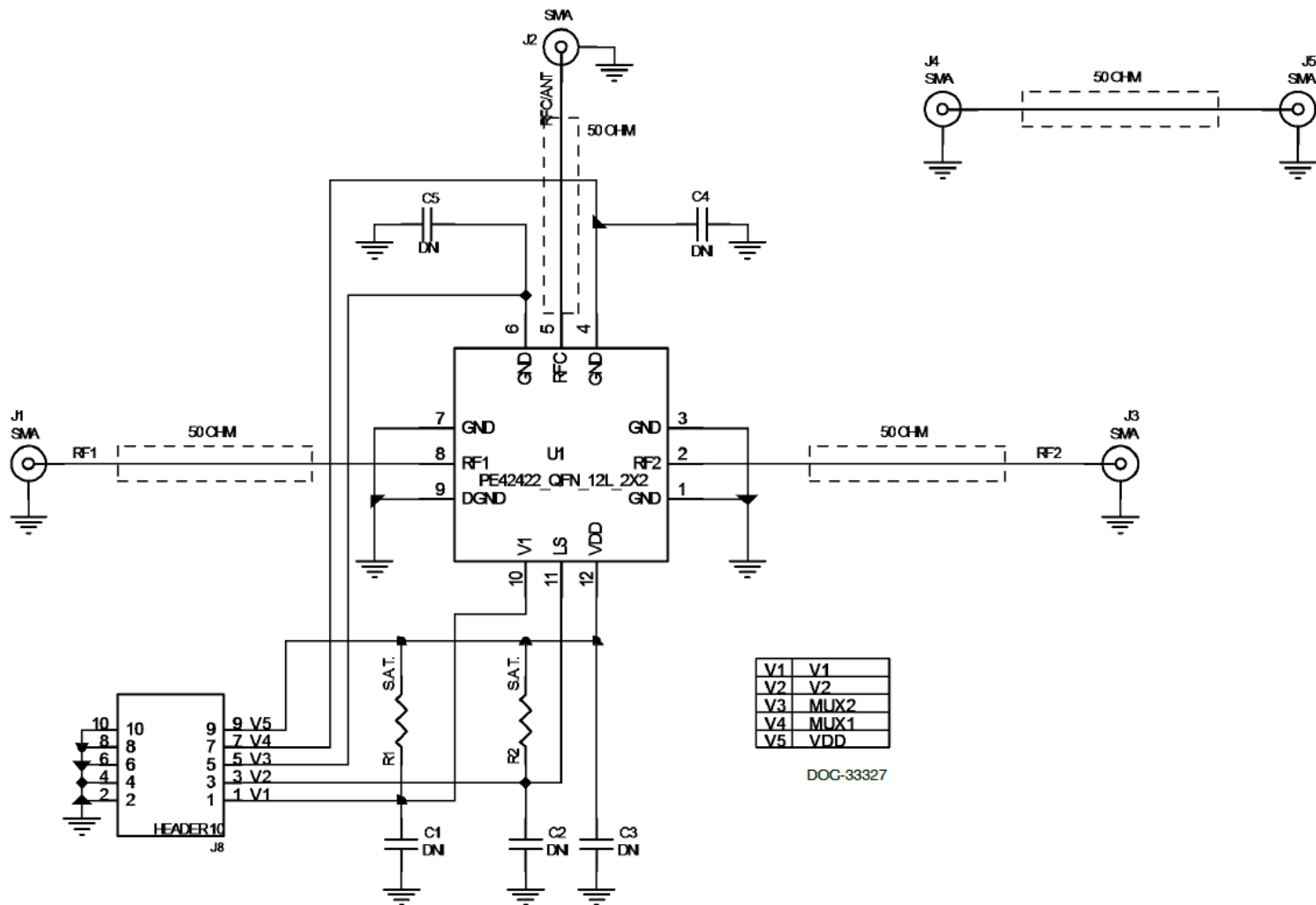


Figure 27. Evaluation board schematic

Figure 28 shows the evaluation board schematic with matching.

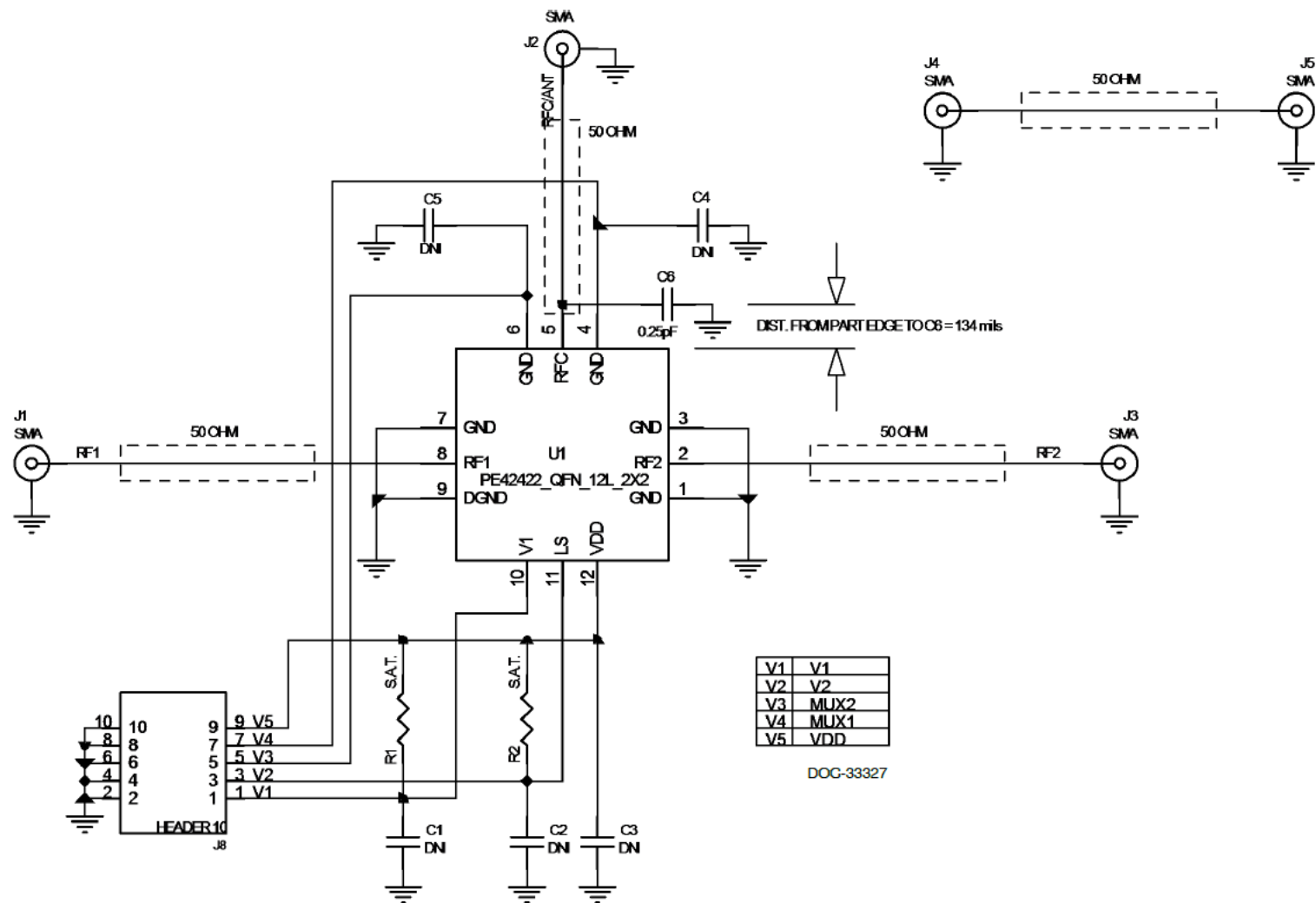


Figure 28. Evaluation board schematic with matching

Pin information

Figure 29 shows the PE42422 pin map for the 12-lead 2 × 2 × 0.55 mm QFN package, and Table 5 lists the description for each pin.

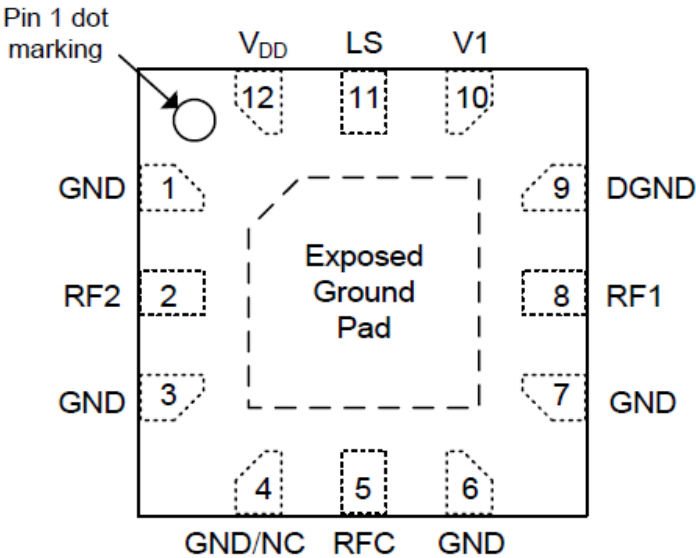


Figure 29. Pin configuration (top view)

Table 5. PE42422 pin descriptions

Pin no.	Pin name	Description
1	GND	Ground
2	RF2 ⁽¹⁾	RF port 2
3	GND	Ground
4	GND/NC ⁽²⁾	Ground or no connect
5	RFc ⁽¹⁾	RF common
6	GND	Ground
7	GND	Ground
8	RF1 ⁽¹⁾	RF port 1
9	DGND	Digital ground
10	V1	Switch control input, CMOS logic level
11	LS	Logic Select, CMOS logic level
12	VDD	Supply
Pad	GND	Exposed pad. Ground for proper operation.

- 1. RF pins 2, 5, and 8 must all be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
- 2. Pin 4 can be grounded or left unconnected externally.

Packaging information

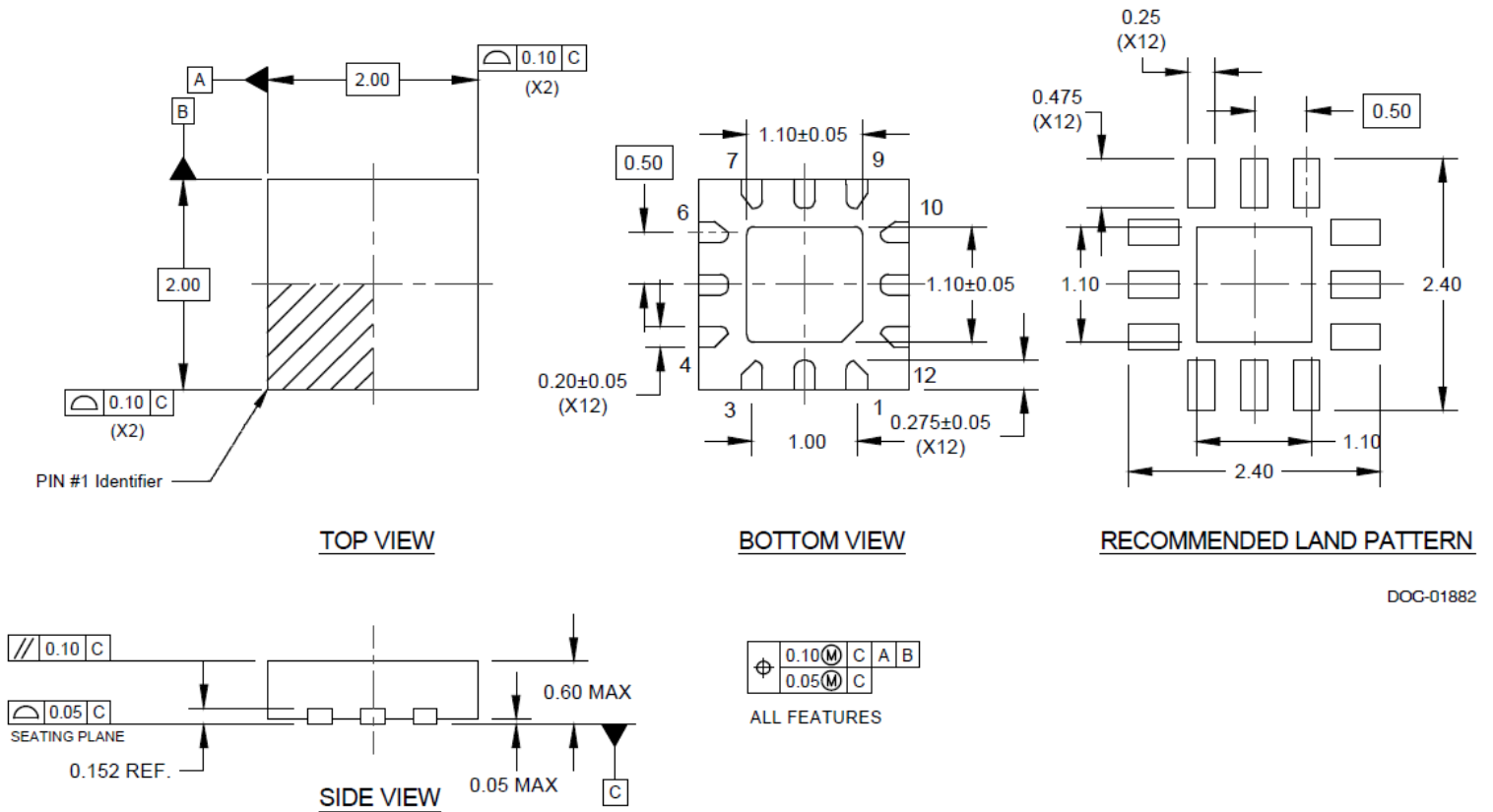
This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42422 moisture sensitivity level rating for the 12-lead $2 \times 2 \times 0.55$ mm QFN package is MSL1.

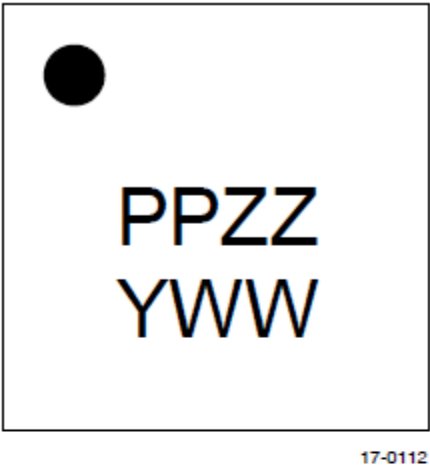
Package drawing



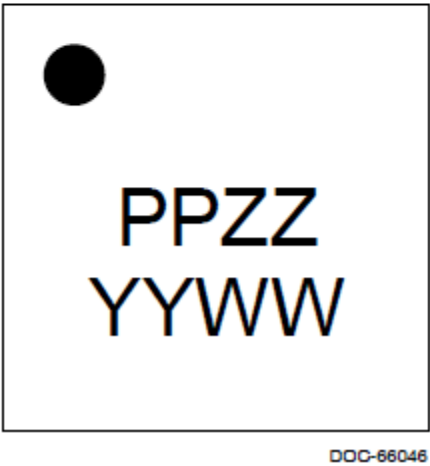
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Figure 30. Package mechanical drawing for the 12-lead $2 \times 2 \times 0.55$ mm QFN package

Top-marking specifications



Marking Spec Symbol	Package Marking	Definition
PP	DE	Part number marking for PE42422
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week



Marking Spec Symbol	Package Marking	Definition
PP	DE	Part number marking for PE42422
ZZ	00-99	Last two digits of lot code
YY	00-99	Last two digits of assembly year (Ex: 15 for 2015)
WW	01-53	Work week

Figure 31. PE42422 package marking specifications

Tape and reel specification

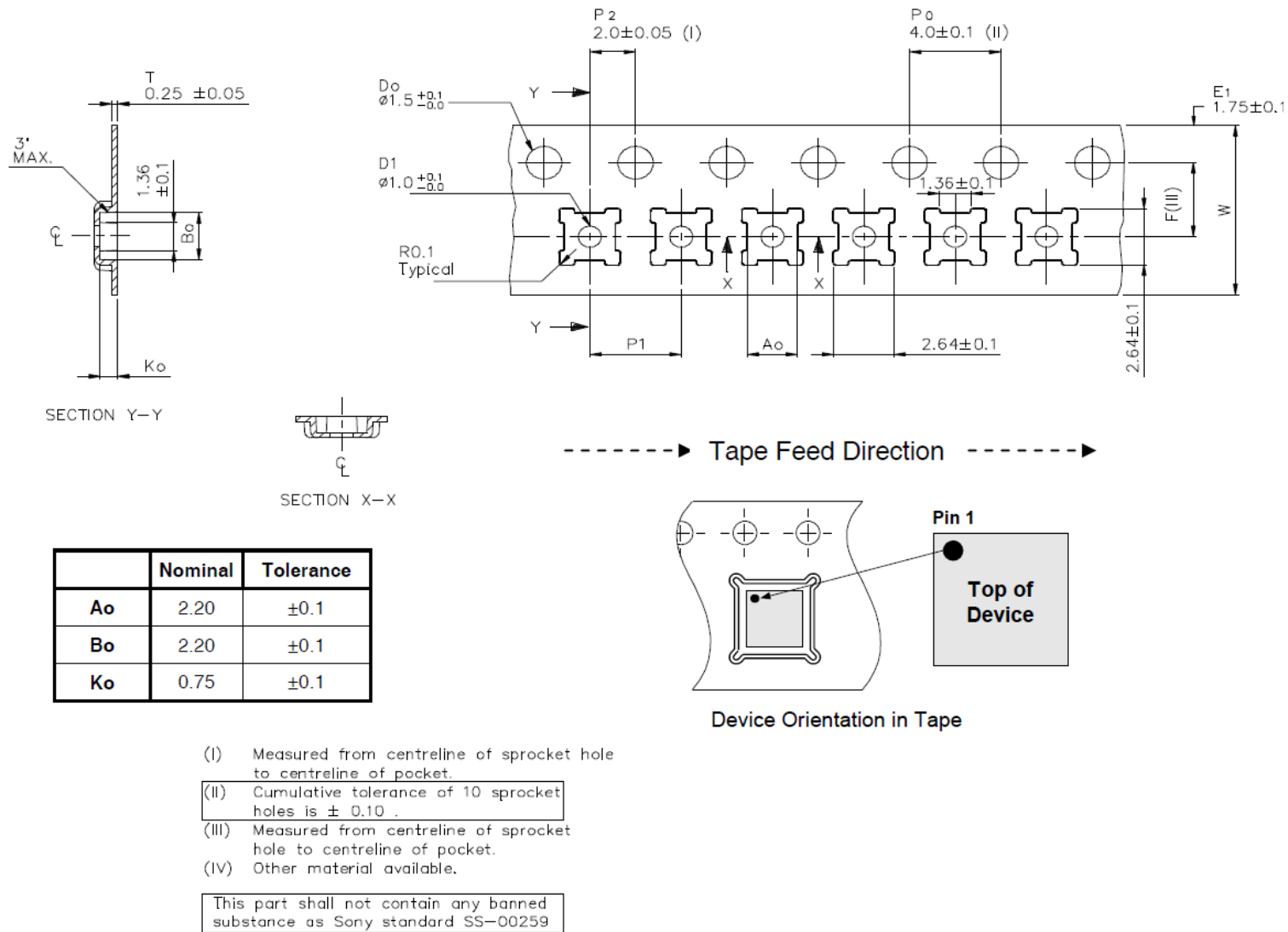


Figure 32. Tape and reel specification for the 12-lead 2 × 2 × 0.55 mm QFN package

Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42422MLAA-Z	PE42422 SPDT RF switch	Green 12-lead 2 × 2mm QFN	3000 units/T&R
EK42422-01	PE42422 evaluation board	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com .

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