PE42423

Document category: Product Specification

UltraCMOS® SPDT RF Switch, 100 MHz–8.5 GHz

Features

- 802.11 a/b/g/n/ac support
- Wide supply range: 2.3–5.5V
- +1.8V control logic compatible
- Exceptional isolation:
  - 47 dB @ 2.4 GHz
  - 43 dB @ 6.0 GHz
- High linearity across supply range:
  - IIP3 of 65 dBm
  - IIP2 of 120 dBm
- High power handling:
  - 38.5 dBm @ 2.4 GHz
  - 37.0 dBm @ 6.0 GHz
- Fast switching time: 500 ns
- ESD performance:
  - 3 kV HBM on RF pins to GND
  - 1.5 kV HBM on all pins
  - 1 kV CDM on all pins
- Packaging: 16-lead 3 × 3 mm QFN

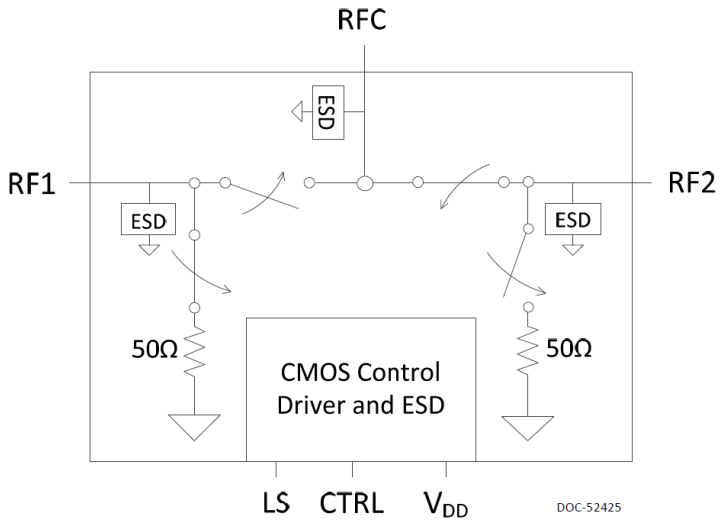

Figure 1. PE42423 functional diagram

Product description

The PE42423 is a HaRP™ technology-enhanced absorptive 50Ω SPDT RF switch designed for use in high-power and high-performance WLAN 802.11 a/b/g/n/ac applications—such as carrier and enterprise Wi-Fi® Products—supporting bandwidths up to 8.5 GHz.

This switch features high linearity that remains invariant across the full supply range. The PE42423 also features exceptional isolation, high power handling and is offered in a 16-lead 3 × 3 mm QFN package. No external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42423 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42423 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage, CTRL	V_{CTRL}	-0.3	3.6	V
LS input voltage	V_{LS}	-0.3	3.6	V
Maximum input power: - 0.1–0.6 GHz - 0.6–4.0 GHz - 4.0–8.50 GHz	$P_{MAX,ABS}$	–	 30 39 37.5	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM:(1) - RF pins to GND - All pins	$V_{ESD,HBM}$	–	 3000 1500	V
ESD voltage MM, all pins(2)	$V_{ESD,MM}$	–	200	V
ESD voltage CDM, all pins(3)	$V_{ESD,CDM}$	–	1000	V

1. Human Body Model (MIL-STD 883 Method 3015).
2. Machine Model (JEDEC JESD22-A115).
3. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE42423 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42423 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	120	200	µA
Digital input high, CTRL	V_{IH}	1.17	–	3.6	V
Digital input low, CTRL	V_{IL}	-0.3	–	0.6	V
RF input power, CW: - 0.1–0.6 GHz - 0.6–4.0 GHz - 4.0–8.50 GHz	$P_{MAX,CW}$	–	–	27 Figure 2 Figure 2	dBm
RF input power, pulsed:(*) - 0.1–0.6 GHz - 0.6–4.0 GHz - 4.0–8.50 GHz	$P_{MAX,PULSED}$	–	–	27 Figure 2 Figure 2	dBm
RF input power into terminated ports, CW	$P_{MAX,TERM}$	–	–	22	dBm
Operating temperature range	T_{OP}	-40	+25	+125	°C

* Pulsed, 5% duty cycle of 4620-µs period, 50Ω.

Electrical specifications

Table 3 lists the PE42423 key electrical specifications at +25 °C and V_{DD} = 3.3V, unless otherwise specified.

Table 3. PE42423 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	0.1	–	8.5	GHz
Insertion loss	RFC–RFx	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz 6.0–8.5 GHz	–	0.80 0.95 0.95 1.1	1.0 1.1 1.1 1.3	dB
Isolation	RFx–RFx	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz 6.0–8.5 GHz	49 39 39 33	51 41 41 35	–	dB
Isolation	RFC–RFx	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz 6.0–8.5 GHz	44 39 40 37	47 41 43 42	–	dB
Return loss (common and active port)	RFx	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz 6.0–8.5 GHz	–	19 16 16 16	–	dB
Return loss (terminated port)	RFx	0.1–2.4 GHz 2.4–5.8 GHz 5.8–6.0 GHz 6.0–8.5 GHz	–	23 23 24 15	–	dB
Input 0.1-dB compression point[1]	RFC–RFx	0.6–4.0 GHz	–	39.5	–	dBm
Input IP3[2]	RFC–RFx	0.8–2.7 GHz	–	65	–	dBm
Input IP2[2]	RFC–RFx	0.8–2.7 GHz	–	120	–	dBm
Switching time[3]	–	50% CTRL to 90% or 10% of final value	–	500	700	ns

1. The input 0.1-dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
2. The input intercept point remains invariant over the full supply range as defined in Table 2.
3. The PE42423 has a maximum 25 kHz switching rate. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

SPDT control logic

Table 4. PE42423 truth table

LS	CTRL	RFC–RF1	RFC–RF2
0	0	OFF	ON
0	1	ON	OFF
1	0	ON	OFF
1	1	OFF	ON

Logic Select (LS)

The Logic Select (pin 15) determines the definition for the CTRL pin (pin 14).

Power de-rating curve

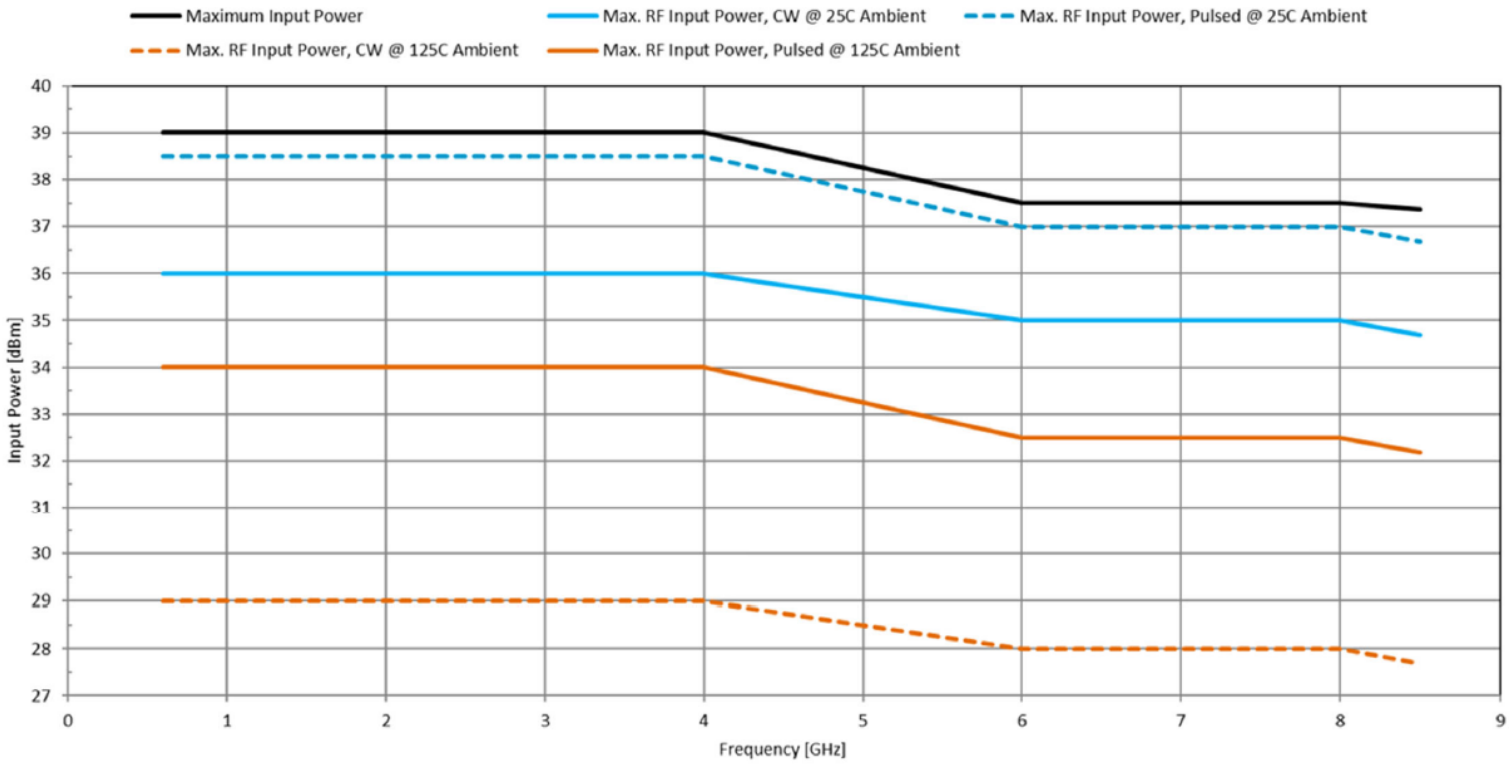


Figure 2. Power de-rating curve up to 8.5 GHz at +125 °C

Typical performance data

Figure 3–Figure 12 show the typical performance data at +25 °C and V_{DD} = 3.3V, unless otherwise specified.

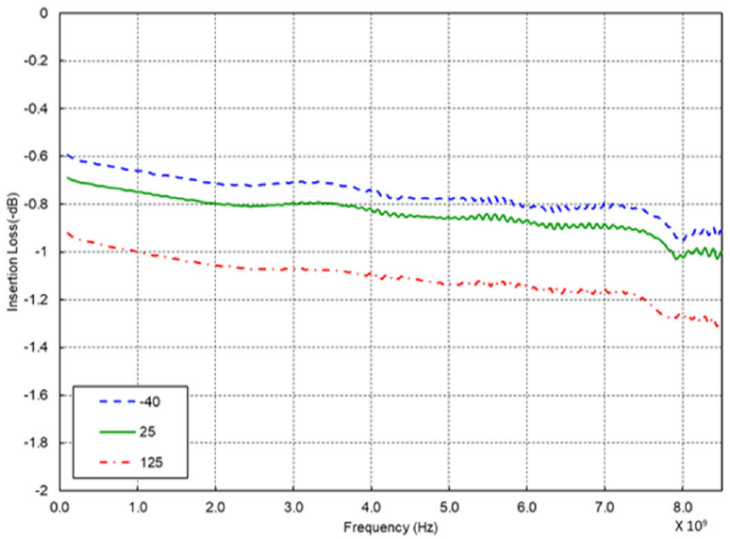


Figure 3. Insertion loss vs. temperature (RFC–RFx)

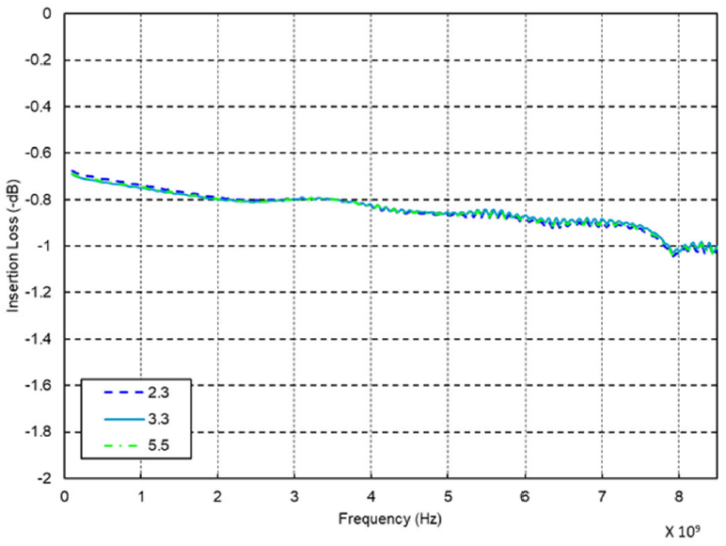


Figure 4. Insertion loss vs. V_{DD} (RFC–RFx)

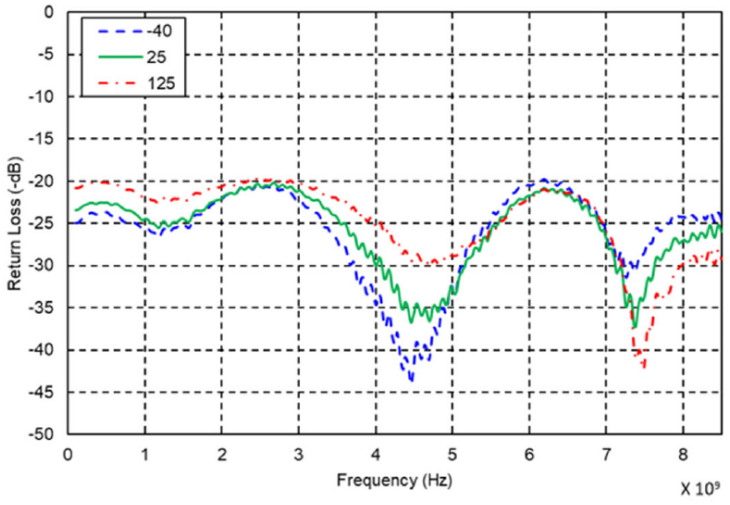


Figure 5. RFx port return loss vs. temperature

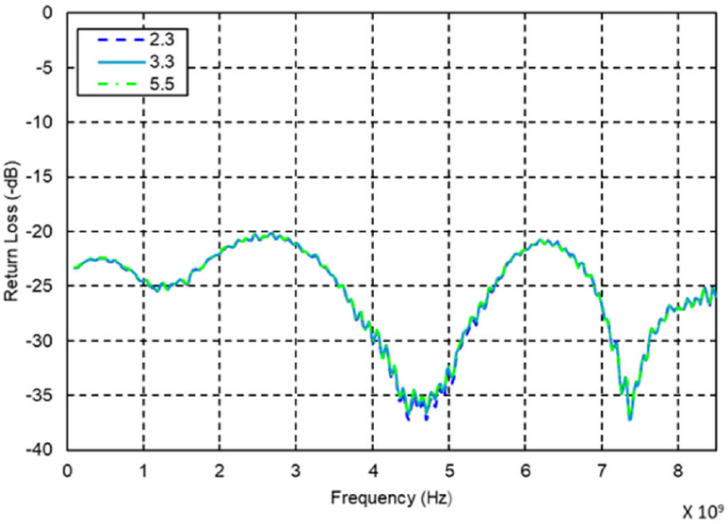


Figure 6. RFx port return loss vs. V_{DD}

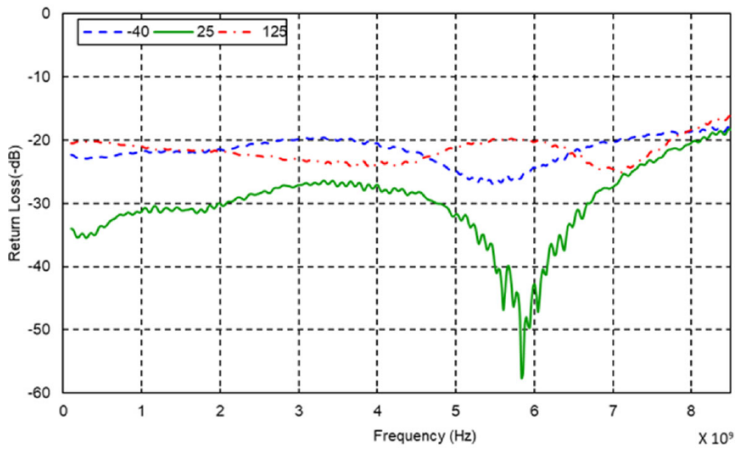


Figure 7. Terminated port return loss vs. temperature

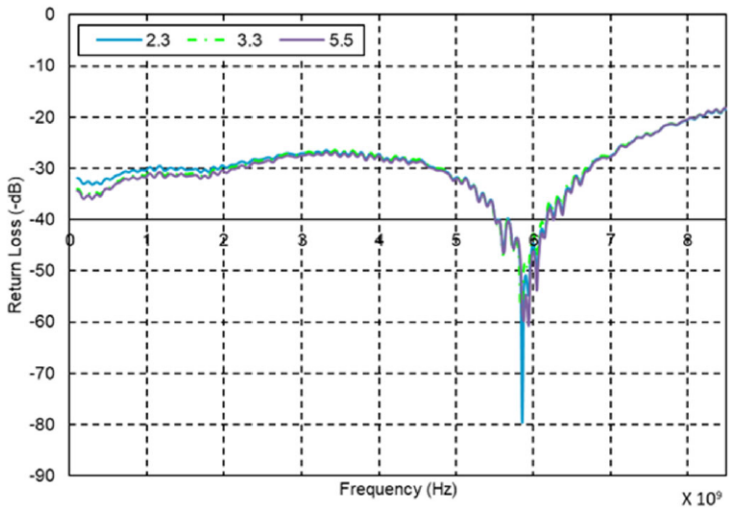


Figure 8. Terminated port return loss vs. V_{DD}

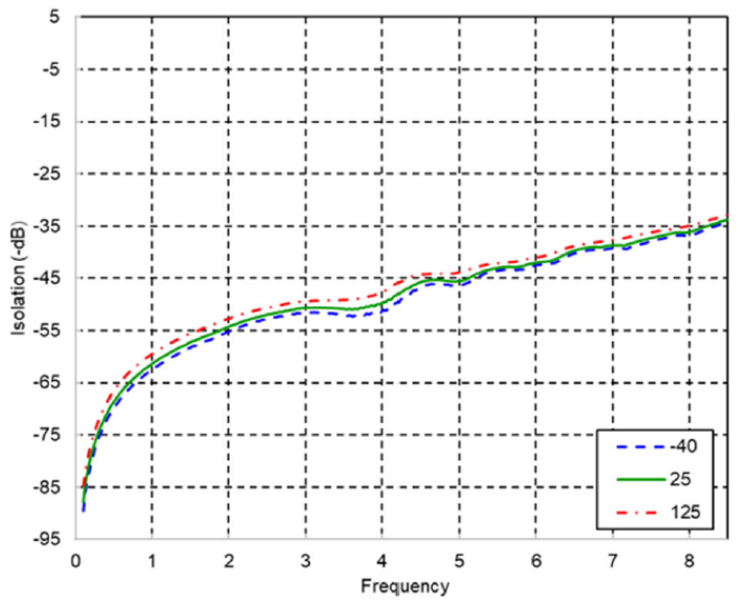


Figure 9. Isolation vs. temperature (RFx–RFx, RFx active)

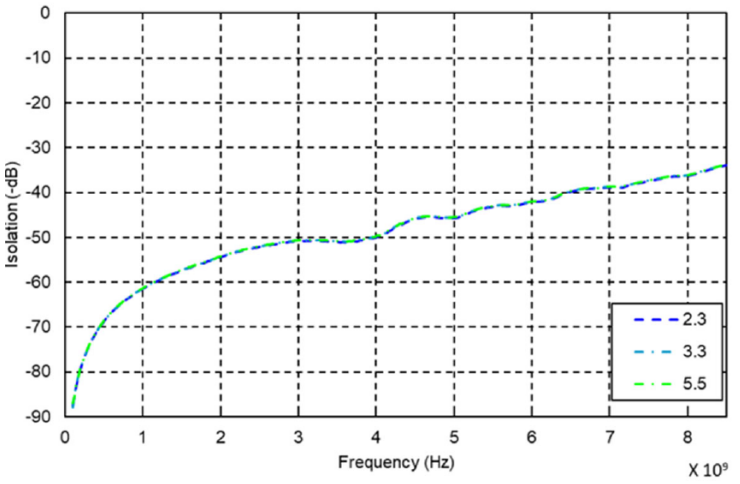


Figure 10. Isolation vs. V_{DD} (RFx–RFx, RFx active)

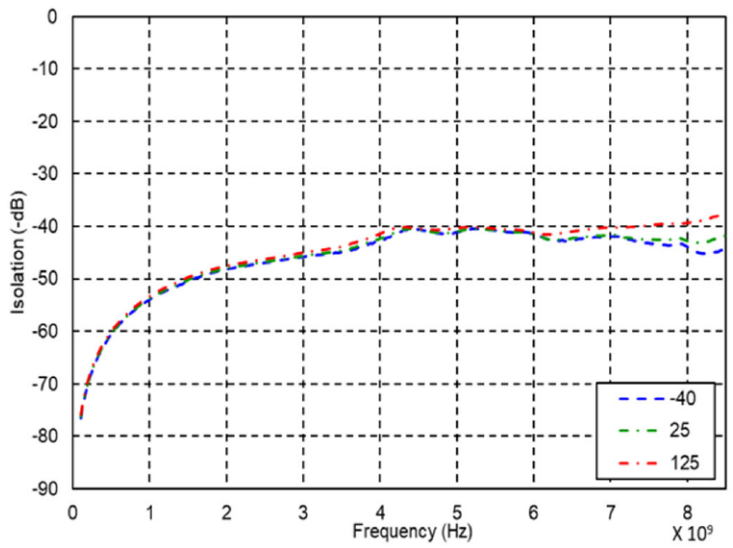


Figure 11. Isolation vs. temperature (RFC–RFx, RFx active)

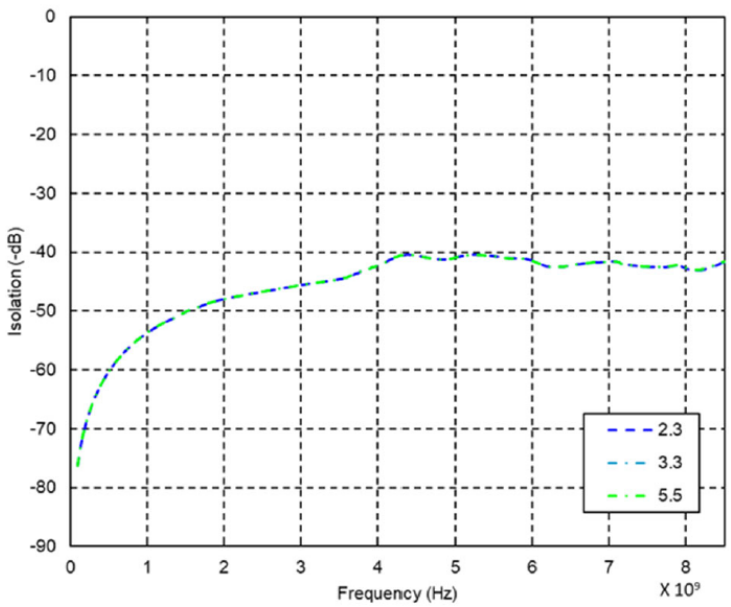


Figure 12. Isolation vs. V_{DD} (RFC–RFx, RFx active)

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the pSemi PE42423. The RF common port connects through a 50Ω transmission line via the SMA connector, J1. The RF1 and RF2 ports connect through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which you can use to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

To realize the true performance of the PE42423, design the PCB so that the RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

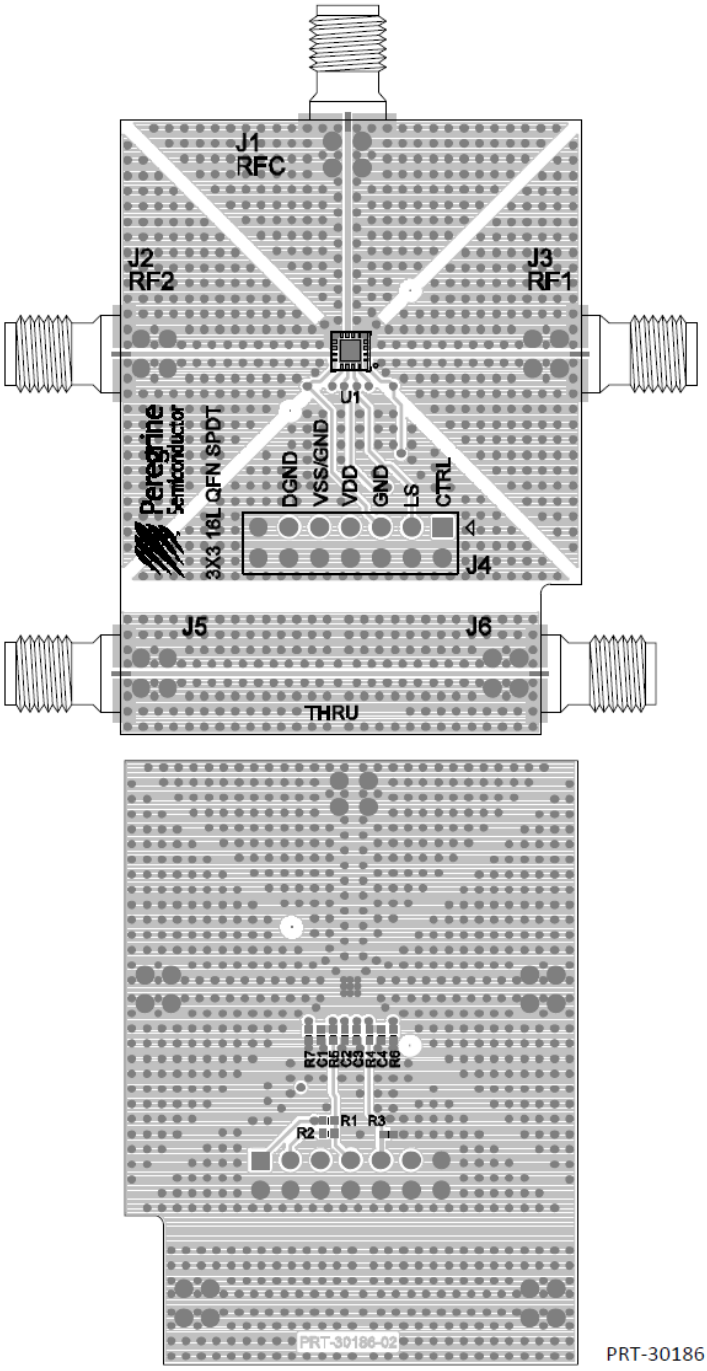
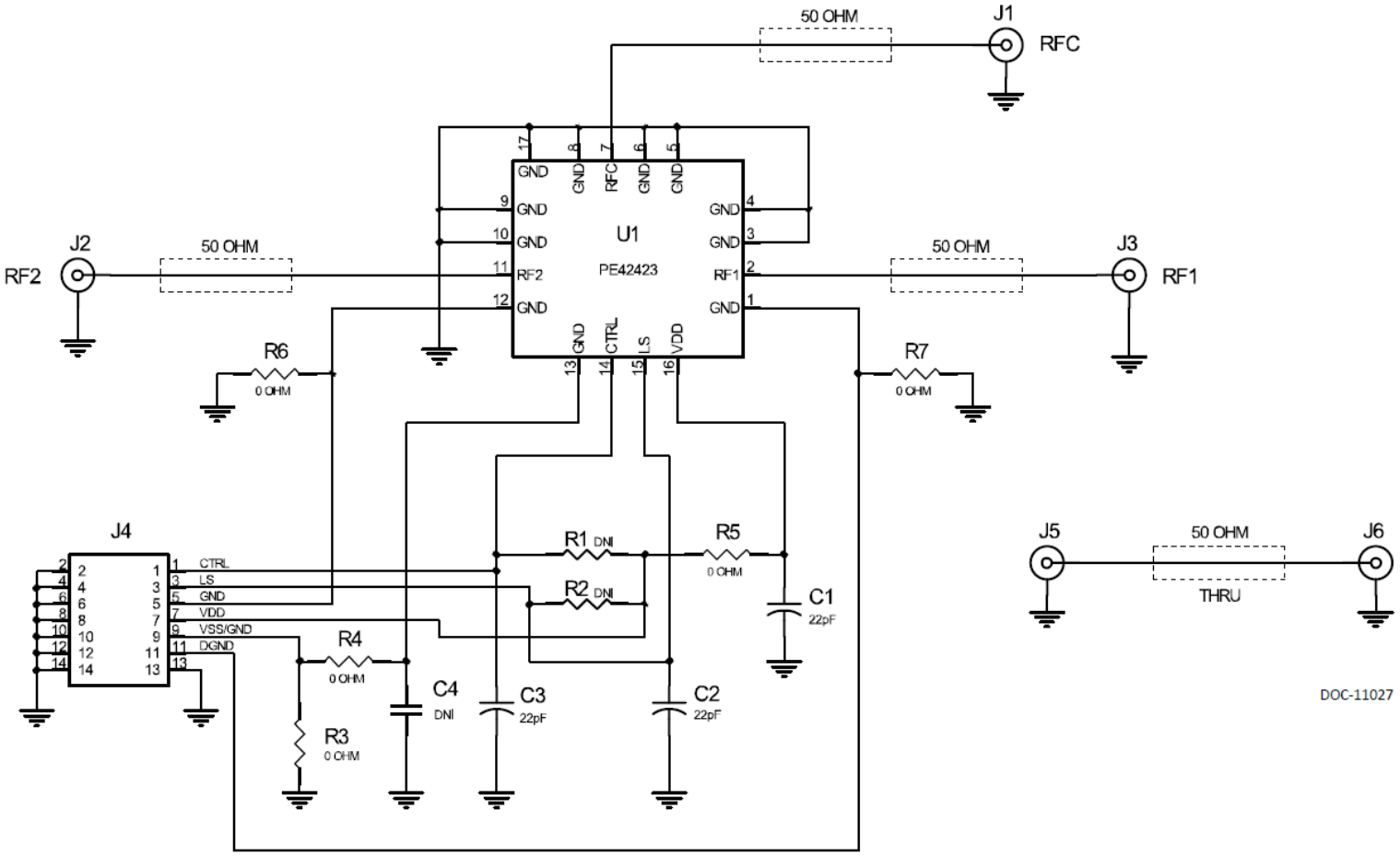


Figure 13. Evaluation board layout

Evaluation board schematic



Notes: 1. Use PRT-30186-2 PCB
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)

Figure 14. Evaluation board schematic

Pin information

Figure 15 shows the PE42423 pin map for the 16-lead 3 × 3 mm QFN package, and Table 5 lists the description for each pin.

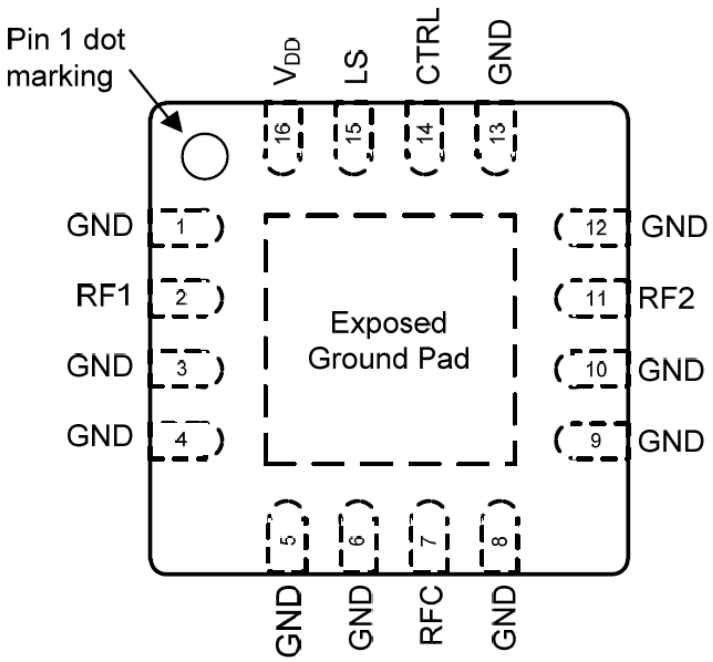


Figure 15. Pin configuration (top view)

Table 5. PE42423 pin descriptions

Pin no.	Pin name	Description
1, 3, 4, 5, 6, 8, 9, 10, 12, 13	GND	Ground
2(*)	RF1	RF port 1
7(*)	RFC	RF common
11(*)	RF2	RF port 2
14	CTRL	Digital control logic input
15	LS	Logic Select: Determines the definition for the CTRL pin. See Table 1.
16	V_{DD}	Supply voltage (nominal 3.3V)
Pad	GND	Exposed pad. Ground for proper operation.

* RF pins 2, 7, and 11 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42423 moisture sensitivity level rating for the 16-lead 3 × 3 mm QFN package is MSL3.

Package drawing

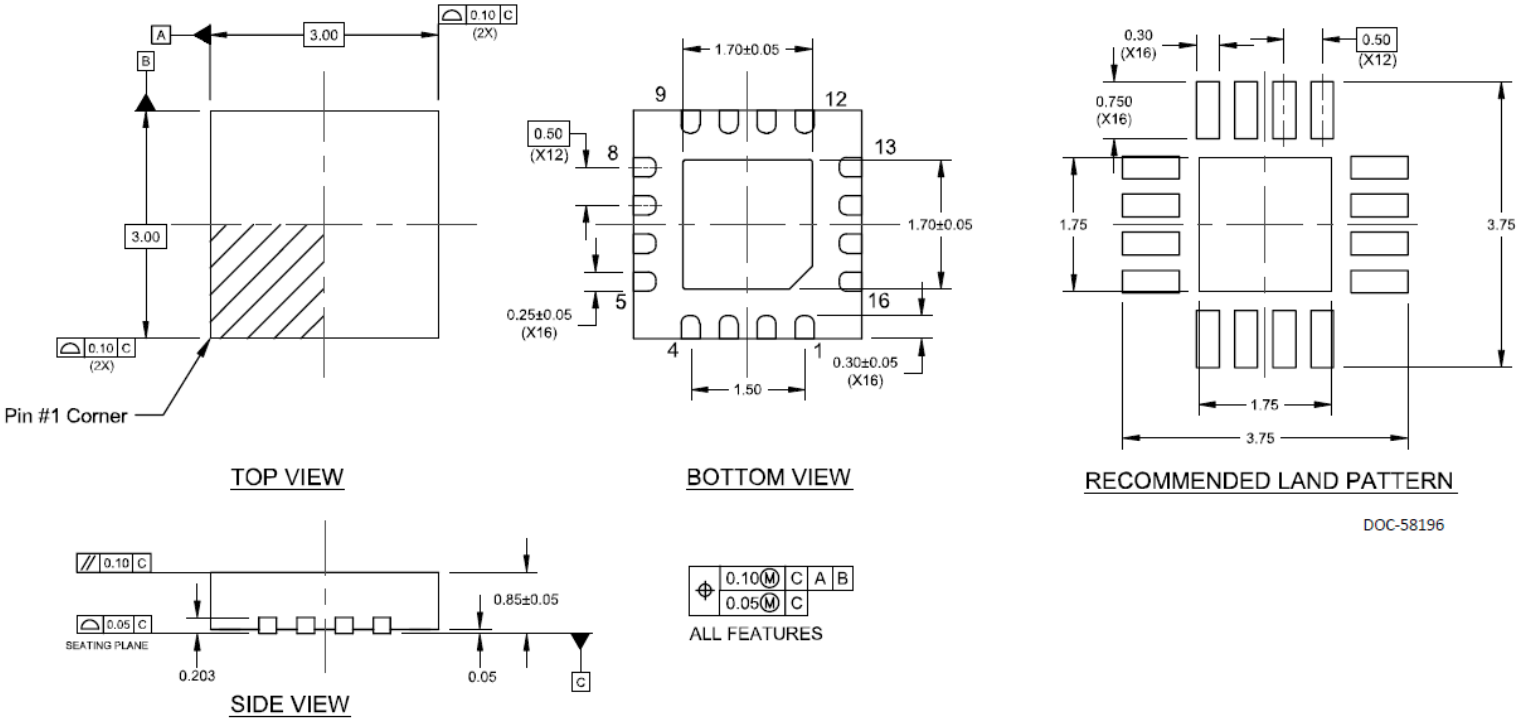


Figure 16. Package mechanical drawing for the 16-lead 3 × 3 mm QFN package

Top-marking specification

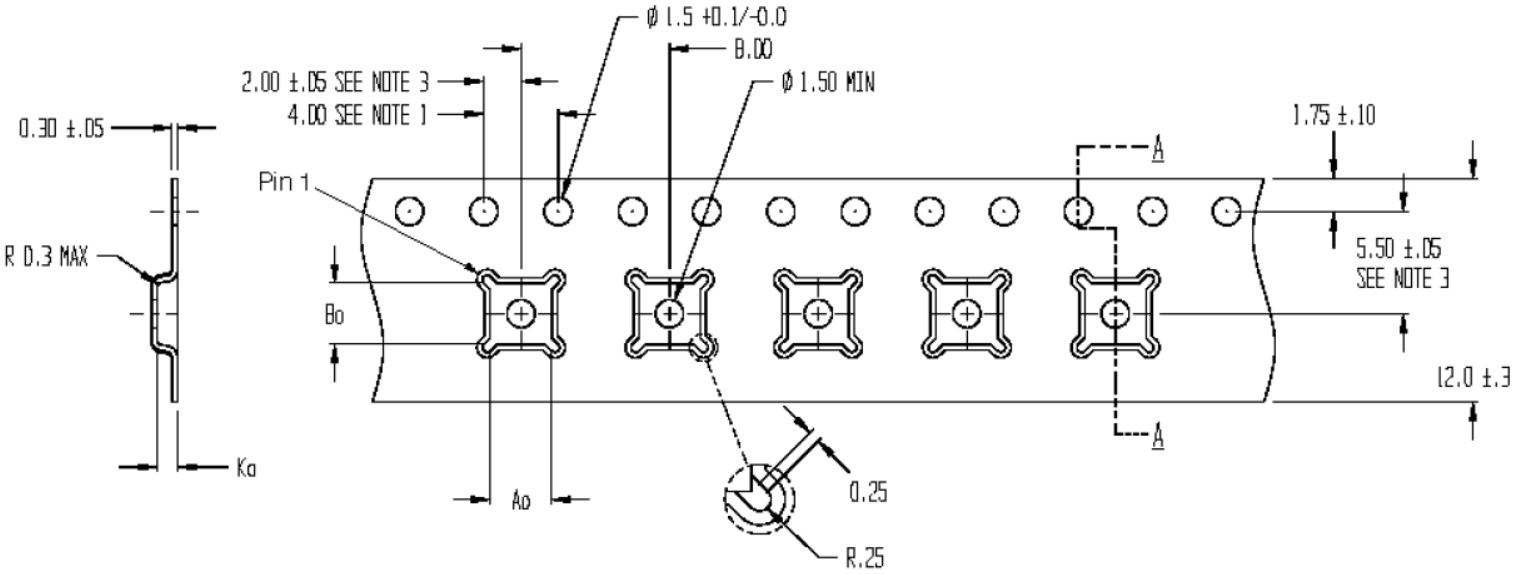
● = Pin 1 designator

YYWW = Assembly year and work week date code

ZZZZZZ = Last six characters of assembly lot code

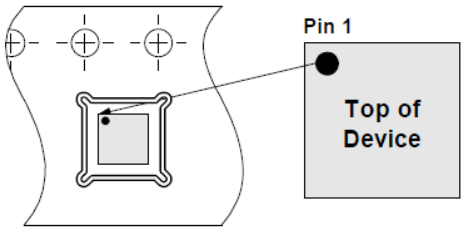
Figure 17. PE42423 package marking specification

Tape and reel specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 3.30
Bo = 3.30
Ko = 1.10



Device Orientation in Tape

Figure 18. Tape and reel specification for the 16-lead 3 × 3 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE42423B-Z	PE42423 SPDT RF switch	Green 16-lead 3 × 3 mm QFN	3000 units/T&R
EK42423-03	PE42423 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

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