# PE43704

## Document category: Product Specification

*UltraCMOS® RF Digital Step Attenuator, 7-bit, 31.75 dB, 9 kHz–8 GHz*

## Features

- HaRP™ technology enhanced
- Safe attenuation state transitions
- Attenuation options: covers a 31.75 dB range in 0.25-dB, 0.5-dB, or 1.0-dB steps:
  - 0.25 dB monotonicity for ≤ 6 GHz
  - 0.50 dB monotonicity for ≤ 7 GHz
  - 1.00 dB monotonicity for ≤ 8 GHz
- High power handling @ 8 GHz in 50Ω:
  - 28 dBm CW
  - 31 dBm instantaneous power
- High linearity: IIP3 of 61 dBm
- 1.8V/3.3V control logic
- Programming modes:
  - Direct parallel
  - Latched parallel
  - Serial
  - Serial addressable
- High-attenuation state at power-up (PUP)
- ESD performance: 1.5 kV HBM on all pins
- Packaging: 32-lead 5×5 QFN

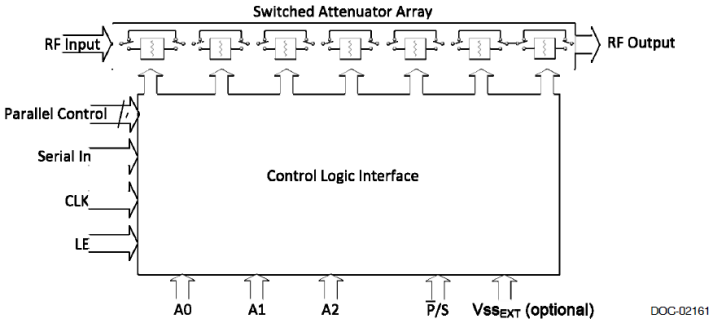



*Figure 1. PE43704 functional diagram*

## Product description

The PE43704 is a HaRP™ technology-enhanced, high linearity, 7-bit 50Ω RF digital step attenuator (DSA). It offers maximum power handling of 28 dBm up to 8 GHz and covers a 31.75 dB attenuation range in 0.25-dB, 0.5-dB, or 1.0-dB steps. The PE43704 is a pin-compatible version of the pSemi PE43703. It provides multiple CMOS control interfaces and an optional $Vss_{EXT}$ bypass mode to improve spurious performance. It maintains high attenuation accuracy over frequency and temperature and exhibits extremely low insertion loss and low power consumption. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE43704 is manufactured using the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

# Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

## ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

## Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE43704 absolute maximum ratings

| Parameter or condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | -0.3 | 5.5 | V |
| Digital input voltage | $V_{CTRL}$ | -0.3 | 3.6 | V |
| RF input power, maximum:<br>- 9 kHz < 50 MHz<br>- 50 MHz ≤ 8 GHz | $P_{MAX,ABS}$ | – | See Figure 4<br>+34 | dBm |
| Storage temperature range | $T_{ST}$ | -65 | +150 | °C |
| ESD voltage HBM, all pins(1) | $V_{ESD,HBM}$ | – | 1500 | V |
| ESD voltage MM, all pins(2) | $V_{ESD,MM}$ | – | 200 | V |
| ESD voltage CDM, all pins(3) | $V_{ESD,CDM}$ | – | 250 | V |

1. Human Body Model (MIL-STD 883 Method 3015).
2. Machine Model (JEDEC JESD22-A115).
3. Charged Device Model (JEDEC JESD22-C101).

# Recommended operating conditions

Table 2 lists the PE43704 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE43704 operating conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage (normal mode, $Vss_{EXT}$ = 0V)(1) | $V_{DD}$ | 2.3 | – | 5.5 | V |
| Supply voltage (bypass mode, $Vss_{EXT}$ = -3.4V, VDD ≥ 3.4V for full spec. compliance)(2) | $V_{DD}$ | 2.7 | 3.4 | 5.5 | V |
| Negative supply voltage (bypass mode)(2) | $Vss_{EXT}$ | -3.6 | – | -2.4 | V |
| Supply current (normal mode, $Vss_{EXT}$ = 0V)(1) | $I_{DD}$ | – | 130 | 200 | µA |
| Supply current (bypass mode, $Vss_{EXT}$ = -3.4V)(2) | $I_{DD}$ | – | 50 | 80 | µA |
| Negative supply current (bypass mode, $Vss_{EXT}$ = -3.4V)(2) | $I_{SS}$ | -40 | -16 | – | µA |
| Digital input high | $V_{IH}$ | 1.17 | – | 3.6 | V |
| Digital input low | $V_{IL}$ | -0.3 | – | 0.6 | V |
| Digital input current | $I_{CTRL}$ | – | – | 15 | µA |
| RF input power, CW:(3)<br>- 9 kHz < 50 MHz<br>- 50 MHz ≤ 8 GHz | $P_{MAX,CW}$ | – | – | See Figure 4<br>+28 | dBm |
| RF input power, pulsed:(4)<br>- 9 kHz < 50 MHz<br>- 50 MHz ≤ 8 GHz | $P_{MAX,PULSED}$ | – | – | See Figure 4<br>+31 | dBm |
| Operating temperature range | $T_{OP}$ | -40 | 25 | +85 | °C |

1. Normal mode: Connect VssEXT (pin 20) to GND (VssEXT = 0V) to enable the internal negative voltage generator.
2. Bypass mode: Use VssEXT (pin 20) to bypass and disable the internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

# Electrical specifications

Table 3 lists the PE43704 key electrical specifications for 0.25-dB steps at +25 °C, $V_{DD}$ = 2.3V to 5.5V, $Vss_{EXT}$ = 0V, or $V_{DD}$ = 3.4V to 5.5V, $Vss_{EXT}$ = -3.4V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 3. PE43704 electrical specifications for 0.25-dB steps

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | – | – | 9 kHz | – | 6000 MHz | As shown |
| Attenuation range | 0.25-dB step | – | – | 0–31.75 | – | dB |
| Insertion loss | – | 9 kHz–2 GHz<br>2 GHz–4 GHz<br>4 GHz–6 GHz | – | 1.3<br>1.7<br>2.4 | 1.6<br>2.0<br>2.8 | dB |
| Attenuation error | 0 dB–15.75 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2% of attenuation setting) | dB |
| | | 4 GHz–6 GHz | – | – | +(0.15 + 6% of attenuation setting)<br>-(0.15 + 1% of attenuation setting) | dB |
| | 16 dB–31.75 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2.5% of attenuation setting) | dB |
| | | 4 GHz–6 GHz | – | – | +(0.25 + 6.5% of attenuation setting)<br>-(0.2 + 1% of attenuation setting) | dB |
| Return loss | Input port | 9 kHz–4 GHz<br>4 GHz–6 GHz | – | 20<br>15 | – | dB |
| | Output port | 9 kHz–4 GHz<br>4 GHz–6 GHz | – | 17<br>13 | – | dB |
| Relative phase | 0 dB–31.75 dB attenuation settings | 9 kHz–6 GHz | – | 58 | – | deg |
| Input 1dB compression point(1) | – | 50 MHz–6 GHz | 32 | 34 | – | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 50 MHz–6 GHz | – | 61 | – | dBm |
| Typical spurious value(2) | $Vss_{EXT}$ = 0V | – | – | -140 | – | dBm |
| RF $T_{RISE}/T_{FALL}$ | 10%/90% RF | – | – | 600 | – | ns |
| Setting time | RF settled to within 0.05 dB of final value | – | – | 2 | – | µs |

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Switching time[3] | 50% CTRL to 90% or 10% RF | – | – | 1.1 | – | µs |

1. The input 1dB compression point is a linearity figure of merit. For the RF input power ($P_{IN}$, 50Ω), see Table 2.
2. To prevent negative voltage generator spurs, supply –3.4 volts to $Vss_{EXT}$.
3. The PE43704 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 20 = GND). The rate at which the PE43704 can switch is only limited to the switching time above if an external negative supply is provided (pin 20 = $Vss_{EXT}$). The switching frequency is the speed at which the DSA can be toggled across attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 4 lists the PE43704 key electrical specifications for 0.5-dB steps at +25 °C, $V_{DD}$ = 2.3V to 5.5V, $Vss_{EXT}$ = 0V, or $V_{DD}$ = 3.4V to 5.5V, $Vss_{EXT}$ = -3.4V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 4. PE43704 electrical specifications for 0.5-dB steps

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | – | – | 9 kHz | – | 7000 MHz | As shown |
| Attenuation range | 0.5-dB step | – | – | 0–31.5 | – | dB |
| Insertion loss | – | 9 kHz–2 GHz<br>2 GHz–4 GHz<br>4 GHz–6 GHz<br>6 GHz–7 GHz | – | 1.3<br>1.7<br>2.4<br>2.5 | 1.6<br>2.0<br>2.8<br>2.9 | dB |
| Attenuation error | 0 dB–15.5 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2% of attenuation setting) | dB |
| | | 4 GHz–7 GHz | – | – | +(0.25 + 5.5% of attenuation setting)<br>-(0.15 + 1% of attenuation setting) | dB |
| | 16 dB–31.5 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2.5% of attenuation setting) | dB |
| | | 4 GHz–7 GHz | – | – | +(0.25 + 6.5% of attenuation setting)<br>-(0.25 + 2.5% of attenuation setting) | dB |
| Return loss | Input port | 9 kHz–4 GHz<br>4 GHz–7 GHz | – | 20<br>16 | – | dB |
| | Output port | 9 kHz–4 GHz<br>4 GHz–7 GHz | – | 17<br>14 | – | dB |
| Relative phase | 0 dB–31.5 dB attenuation settings | 9 kHz–7 GHz | – | 65 | – | deg |
| Input 1dB compression point(1) | – | 50 MHz–7 GHz | 32 | 34 | – | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 50 MHz–7 GHz | – | 61 | – | dBm |
| Typical spurious value(2) | $Vss_{EXT}$ = 0V | – | – | -140 | – | dBm |
| RF $T_{RISE}/T_{FALL}$ | 10%/90% RF | – | – | 600 | – | ns |
| Setting time | RF settled to within 0.05 dB of final value | – | – | 2 | – | µs |
| Switching time(3) | 50% CTRL to 90% or 10% RF | – | – | 1.1 | – | µs |

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

1. The input 1dB compression point is a linearity figure of merit. For the RF input power ($P_{IN}$, 50Ω), see Table 2.
2. To prevent negative voltage generator spurs, supply –3.4 volts to $Vss_{EXT}$.
3. The PE43704 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 20 = GND). The rate at which the PE43704 can switch is only limited to the switching time above if an external negative supply is provided (pin 20 = $Vss_{EXT}$). The switching frequency is the speed at which the DSA can be toggled across attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 5 lists the PE43704 key electrical specifications for 1-dB steps at +25 °C, $V_{DD}$ = 2.3V to 5.5V, $Vss_{EXT}$ = 0V, or $V_{DD}$ = 3.4V to 5.5V, $Vss_{EXT}$ = -3.4V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 5. PE43704 electrical specifications for 1-dB steps

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | – | – | 9 kHz | – | 8000 MHz | As shown |
| Attenuation range | 1-dB step | – | – | 0–31 | – | dB |
| Insertion loss | – | 9 kHz–2 GHz<br>2 GHz–4 GHz<br>4 GHz–6 GHz<br>6 GHz–8 GHz | – | 1.3<br>1.7<br>2.4<br>2.9 | 1.6<br>2.0<br>2.8<br>3.3 | dB |
| Attenuation error | 0 dB–15 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2% of attenuation setting) | dB |
| | | 4 GHz–7 GHz | – | – | +(0.25 + 6% of attenuation setting)<br>-(0.25 + 2% of attenuation setting) | dB |
| | | 7 GHz–8 GHz | – | – | +(0.25 + 7% of attenuation setting)<br>-(0.25 + 2% of attenuation setting) | dB |
| | 16 dB–31 dB attenuation settings | 9 KHz ≤ 4 GHz | – | – | +(0.15 + 4.5% of attenuation setting)<br>-(0.1 + 2.5% of attenuation setting) | dB |
| | | 4 GHz–7 GHz | – | – | +(0.25 + 6.5% of attenuation setting)<br>-(0.25 + 3% of attenuation setting) | dB |
| | | 7 GHz–8 GHz | – | – | +(0.25 + 7% of attenuation setting)<br>-(0.25 + 4% of attenuation setting) | dB |
| Return loss | Input port | 9 kHz–4 GHz<br>4 GHz–8 GHz | – | 20<br>14.5 | – | dB |
| | Output port | 9 kHz–4 GHz<br>4 GHz–8 GHz | – | 17<br>12.5 | – | dB |
| Relative phase | 0 dB–31 dB attenuation settings | 9 kHz–8 GHz | – | 80 | – | deg |
| Input 1dB compression point[1] | – | 50 MHz–8 GHz | 32 | 34 | – | dBm |
| IIP3 | Two tones at +18 dBm, 20 MHz spacing | 50 MHz–8 GHz | – | 61 | – | dBm |
| Typical spurious value[2] | $Vss_{EXT}$ = 0V | – | – | -140 | – | dBm |

| Parameter | Condition | Frequency | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF $T_{RISE}/T_{FALL}$ | 10%/90% RF | – | – | 600 | – | ns |
| Setting time | RF settled to within 0.05 dB of final value | – | – | 2 | – | µs |
| Switching time(3) | 50% CTRL to 90% or 10% RF | – | – | 1.1 | – | µs |

1. The input 1dB compression point is a linearity figure of merit. For the RF input power ($P_{IN}$, 50Ω), see Table 2.
2. To prevent negative voltage generator spurs, supply –3.4 volts to $Vss_{EXT}$.
3. The PE43704 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 20 = GND). The rate at which the PE43704 can switch is only limited to the switching time above if an external negative supply is provided (pin 20 = $Vss_{EXT}$). The switching frequency is the speed at which the DSA can be toggled across attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

## Optional external Vss control ($Vss_{EXT}$)

For proper operation, the VssEXT control pin must be grounded or tied to the Vss voltage specified in Table 2. When the $Vss_{EXT}$ control pin is grounded, FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spur performance, $Vss_{EXT}$ can be applied externally to bypass the internal negative voltage generator.

## Latch and clock specifications

Table 6. Latch and clock specifications

| Latch enable | Shift clock | Function |
|---|---|---|
| 0 | ↑ | Shift register clocked |
| ↑ | X | Contents of the shift register are transferred to the attenuator core. |

## Safe attenuation state transitions

The PE43704 features a novel architecture to ensure safe transition behavior when changing attenuation states. When the RF input power is applied, positive output power spikes are prevented during attenuation state changes by an optimized internal timing control.

# Programming options

## Parallel/serial selection

You can use a parallel or serial-addressable interface to control the PE43704. The P/S bit provides this selection:

- P/S = LOW selects the parallel interface.
- P/S = HIGH selects the serial-addressable interface.

## Parallel interface

The parallel interface consists of seven CMOS-compatible control lines that select the preferred attenuation state, as listed in Table 7.

The parallel interface timing requirements are defined by Figure 3, Table 12, and the switching times in Table 3–Table 5.

For latched-parallel programming, the latch enable (LE) must be held LOW while changing the attenuation state control values, then pulse LE HIGH to LOW (per Figure 3) to latch new attenuation state into device.

For direct parallel programming, the LE line must be pulled HIGH. Changing the attenuation state control values changes the device state to the new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

In parallel mode, the serial-in (SI) and clock (CLK) pins are “don’t care” and can be tied to logic LOW or logic HIGH.

## Serial interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16 bits make up two words consisting of 8-bits each:

- The first word is the *attenuation word*, which controls the state of the DSA.
- The second word is the *address word*, which is compared to the static—or programmed—logical states of the A0, A1, and A2 digital inputs.

If there is an address match, the DSA changes state; otherwise, its current state remains unchanged. Figure 2 shows an example timing diagram for programming a state. All parallel control inputs must be grounded when the DSA is used in serial-addressable mode.

The serial-interface is controlled using three CMOS-compatible signals: serial-in (SI), clock (CLK), and latch enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the attenuation word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input must then be toggled HIGH and brought LOW again, latching the new data into the DSA. Table 8 and Table 9 are the attenuation word and address word truth tables. Table 10 shows a serial register programming example. Figure 2 shows the serial timing diagram.

## Power-up control settings

The PE43704 always initializes to the maximum attenuation setting (31.75 dB) on power-up for both the serial-addressable and latched-parallel modes of operation and remains in this setting until you latch in the next programming word. In direct-parallel mode, the DSA can be preset to any state within the 31.75 dB range by presetting the parallel control pins before power-up. In this mode, there is a 400-µs delay between the time the DSA is powered-up to the time the preferred state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to your defined state. If the control pins are left floating in this mode during power-up, the device defaults to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial and parallel programming modes is possible.
If the DSA powers up in serial mode (P/S = HIGH), all the parallel control inputs DI[6:0] must be set to logic low. Before toggling to parallel mode, the DSA must be programmed serially to ensure that D[7] is set to logic low.

If the DSA powers up in either latched or direct-parallel mode, all parallel pins DI[6:0] must be set to logic low before toggling to serial-addressable mode (P/S = HIGH), and held low until the DSA has been programmed serially to ensure that bit D[7] is set to logic low.

The sequencing is only required once upon power-up. After this is completed, you can toggle the DSA between its serial and parallel programming modes as needed.

# Truth tables

Table 7. Parallel truth table

| Parallel control setting | | | | | | | Attenuation setting RF1–RF2 |
|---|---|---|---|---|---|---|---|
| D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| L | L | L | L | L | L | L | Reference IL |
| L | L | L | L | L | L | H | 0.25 dB |
| L | L | L | L | L | H | L | 0.5 dB |
| L | L | L | L | H | L | L | 1 dB |
| L | L | L | H | L | L | L | 2 dB |
| L | L | H | L | L | L | L | 4 dB |
| L | H | L | L | L | L | L | 8 dB |
| H | L | L | L | L | L | L | 16 dB |
| H | H | H | H | H | H | H | 31.75 dB |

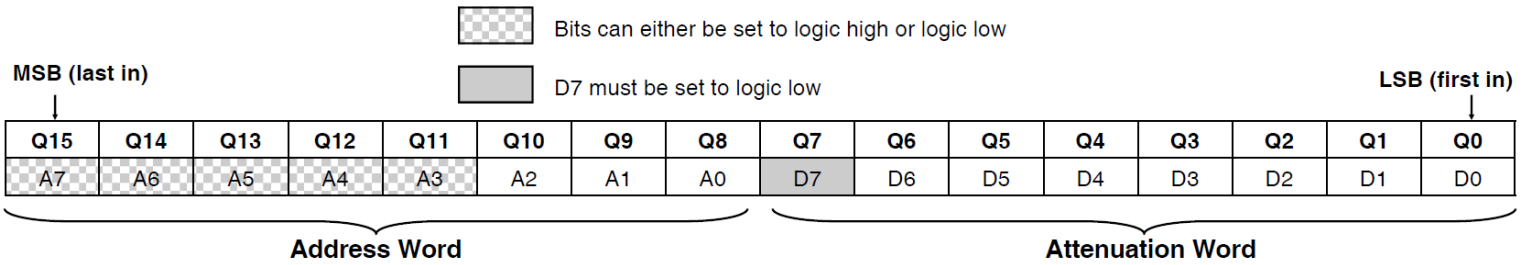
Table 8. Serial attenuation word truth table

| Attenuation word | | | | | | | | Attenuation setting RF1–RF2 |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | |
| L | L | L | L | L | L | L | L | Reference IL |
| L | L | L | L | L | L | L | H | 0.25 dB |
| L | L | L | L | L | L | H | L | 0.5 dB |
| L | L | L | L | L | H | L | L | 1 dB |
| L | L | L | L | H | L | L | L | 2 dB |
| L | L | L | H | L | L | L | L | 4 dB |
| L | L | H | L | L | L | L | L | 8 dB |
| L | H | L | L | L | L | L | L | 16 dB |
| L | H | H | H | H | H | H | H | 31.75 dB |

Table 9. Serial address word truth table

| Address word | | | | | | | | Address setting |
|---|---|---|---|---|---|---|---|---|
| A7 (MSB) | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| X | X | X | X | X | L | L | L | 000 |
| X | X | X | X | X | L | L | H | 001 |
| X | X | X | X | X | L | H | L | 010 |
| X | X | X | X | X | L | H | H | 011 |
| X | X | X | X | X | H | L | L | 100 |
| X | X | X | X | X | H | L | H | 101 |
| X | X | X | X | X | H | H | L | 110 |
| X | X | X | X | X | H | H | H | 111 |

Table 10. Serial-addressable register map




The attenuation word is derived directly from the attenuation value. For example, to program the 18.25 dB state at address 3:

- Address word: XXXXX011
- Attenuation word: Multiply by four and convert to binary → 4 * 18.25 dB → 73 → 01001001
- Serial input: XXXXX01101001001

## Timing diagrams

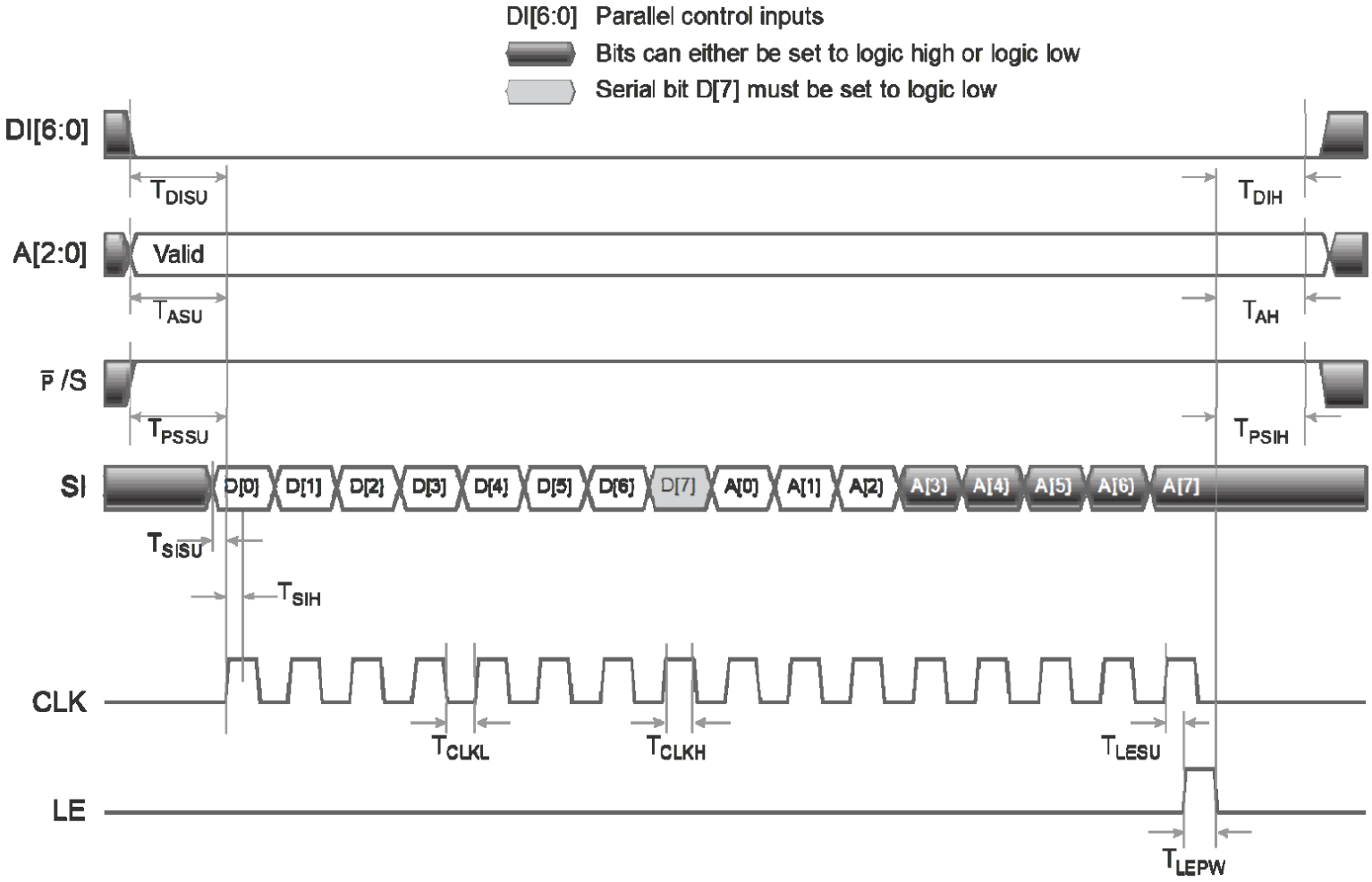



*Figure 2. Serial-addressable timing diagram*

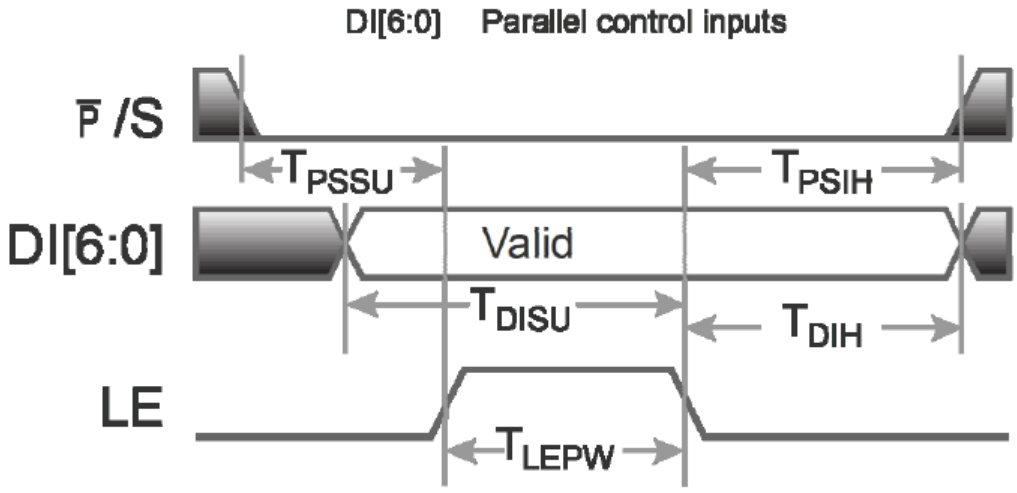



*Figure 3. Latched-parallel/direct-parallel timing diagram*

# AC characteristics

Table 11 lists the PE43704 serial interface AC characteristics for $V_{DD}$ = 3.4V or 5.0V and -40 °C < $T_A$ < 85 °C, unless otherwise specified.

Table 11. Serial interface AC characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Serial clock frequency | $F_{CLK}$ | – | 10 | MHz |
| Serial clock HIGH time | $T_{CLKH}$ | 30 | – | ns |
| Serial clock LOW time | $T_{CLKL}$ | 30 | – | |
| Last serial clock rising edge setup time to Latch Enable rising edge | $T_{LESU}$ | 10 | – | |
| Latch enable minimum pulse width | $T_{LEPW}$ | 30 | – | |
| Serial data setup time | $T_{SISU}$ | 10 | – | |
| Serial data hold time | $T_{SIH}$ | 10 | – | |
| Parallel data setup time | $T_{DISU}$ | 100 | – | |
| Parallel data hold time | $T_{DIH}$ | 100 | – | |
| Address setup time | $T_{ASU}$ | 100 | – | |
| Address hold time | $T_{AH}$ | 100 | – | |
| Parallel/serial setup time | $T_{PSSU}$ | 100 | – | |
| Parallel/serial hold time | $T_{PSIH}$ | 100 | – | |

Table 12 lists the PE43704 parallel and direct interface AC characteristics for $V_{DD}$ = 3.4V or 5.0V and -40 °C < $T_A$ < 85 °C, unless otherwise specified.

Table 12. Parallel and direct interface AC characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Latch enable minimum pulse width | $T_{LEPW}$ | 30 | – | ns |
| Parallel data setup time | $T_{DISU}$ | 100 | – | |
| Parallel data hold time | $T_{DIH}$ | 100 | – | |
| Parallel/serial data setup time | $T_{PSSU}$ | 100 | – | |
| Parallel/serial data hold time | $T_{PSIH}$ | 100 | – | |

# Power de-rating curve

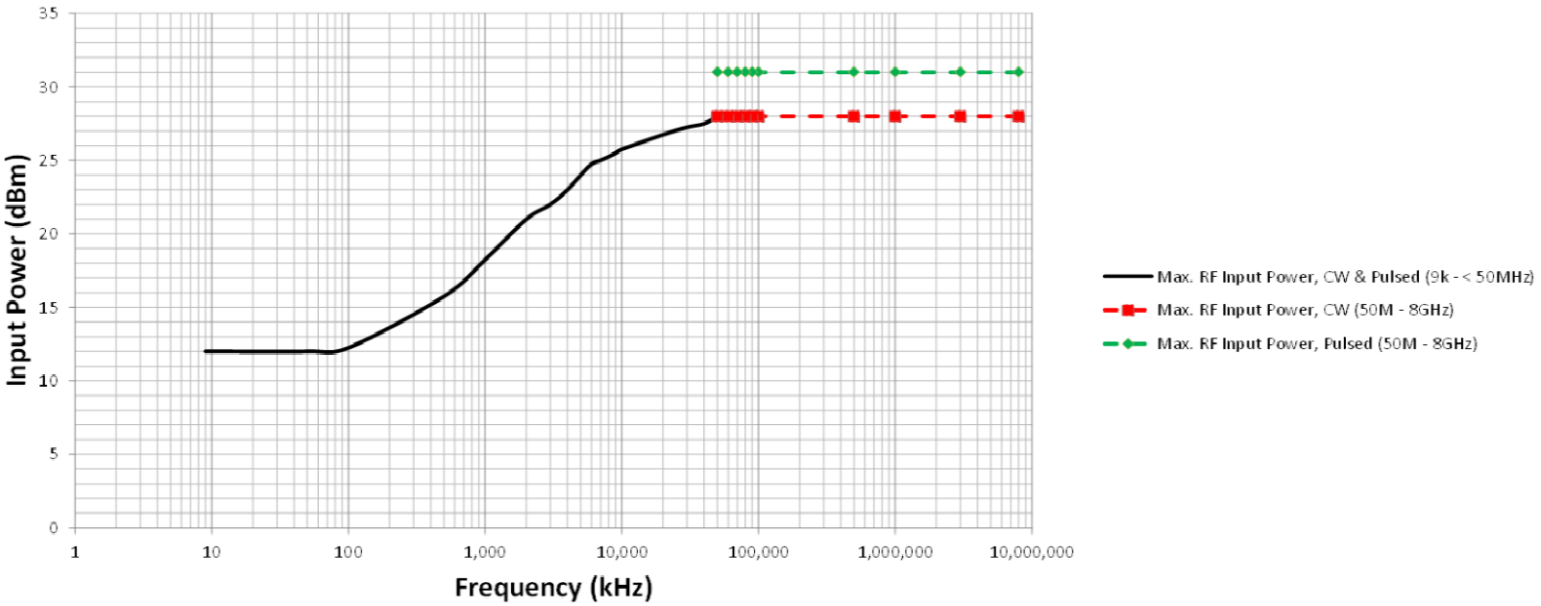



*Figure 4. Power de-rating curve*

# Typical performance data

Figure 5–Figure 8 show the typical performance data for 0.25-dB steps at +25 °C and $V_{DD}$ = 3.4V, unless otherwise specified.

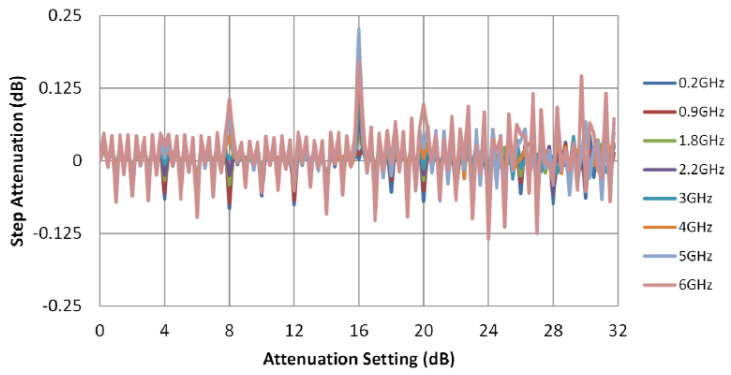



*Figure 5. 0.25-dB step attenuation vs. frequency(*)*

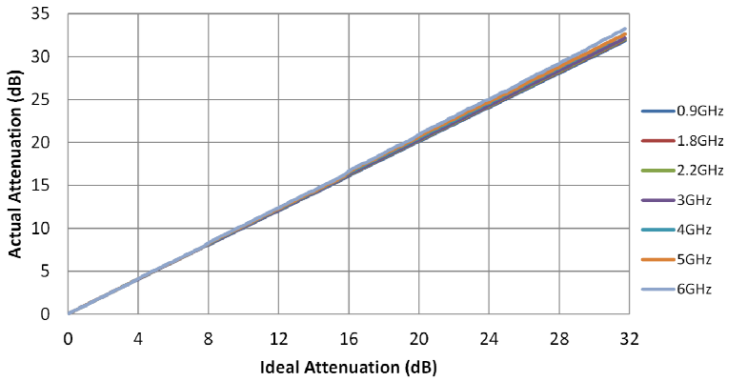



*Figure 6. 0.25-dB step, actual vs. frequency*

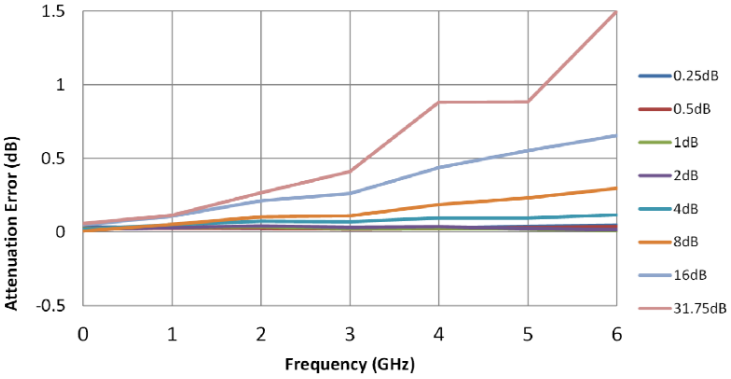



*Figure 7. 0.25-dB major state bit error vs. attenuation setting*

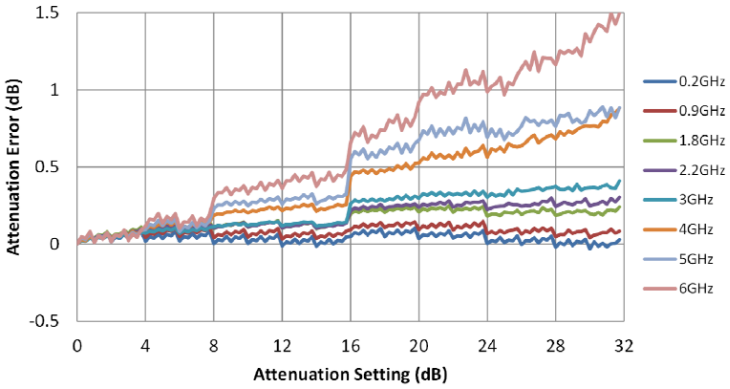



*Figure 8. 0.25-dB attenuation error vs. frequency*

* Monotonicity is held as long as the step-attenuation does not cross below –0.25 dB.

Figure 9–Figure 12 show the typical performance data for 0.5-dB steps at +25 °C and $V_{DD}$ = 3.4V, unless otherwise specified.

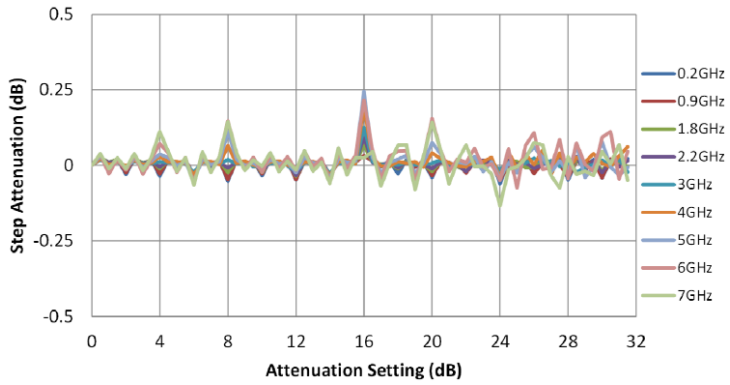



*Figure 9. 0.5-dB step attenuation vs. frequency(*)*

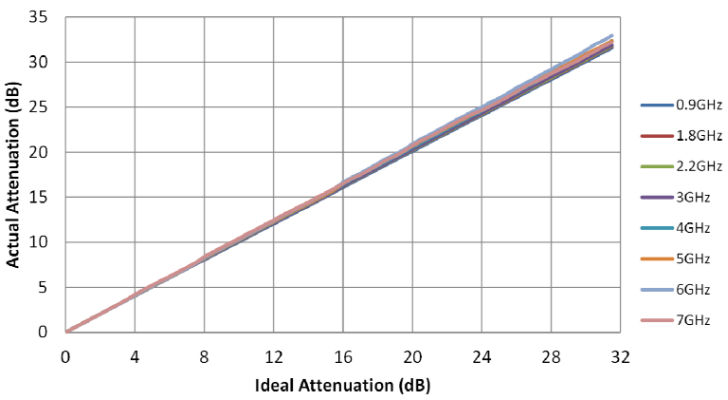



*Figure 10. 0.5-dB step, actual vs. frequency*

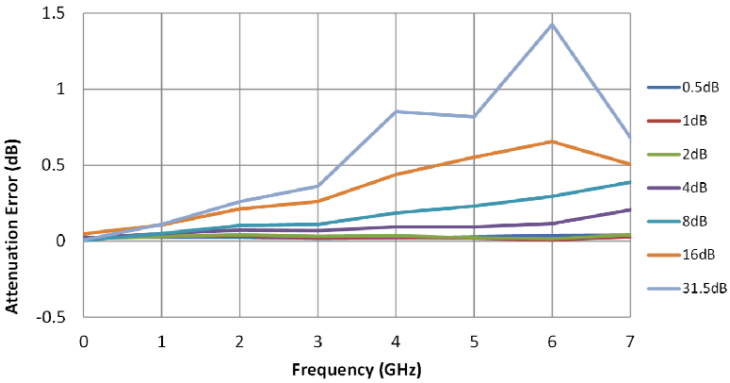



*Figure 11. 0.5-dB major state bit error vs. attenuation setting*

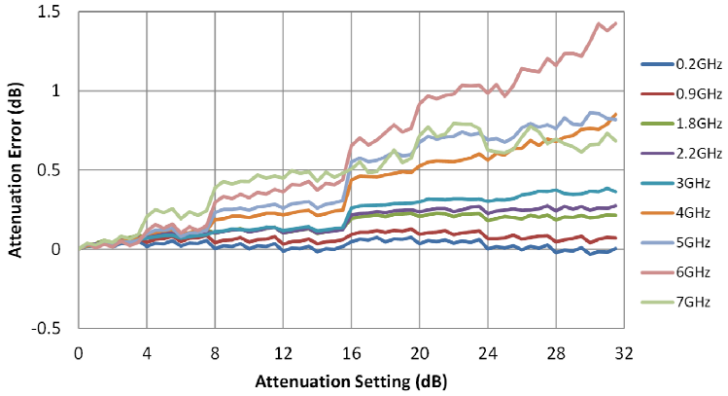



*Figure 12. 0.5-dB attenuation error vs. frequency*

* Monotonicity is held as long as the step-attenuation does not cross below –0.5 dB.

Figure 13–Figure 21 show the typical performance data for 1-dB steps at +25 °C and $V_{DD}$ = 3.4V, unless otherwise specified.

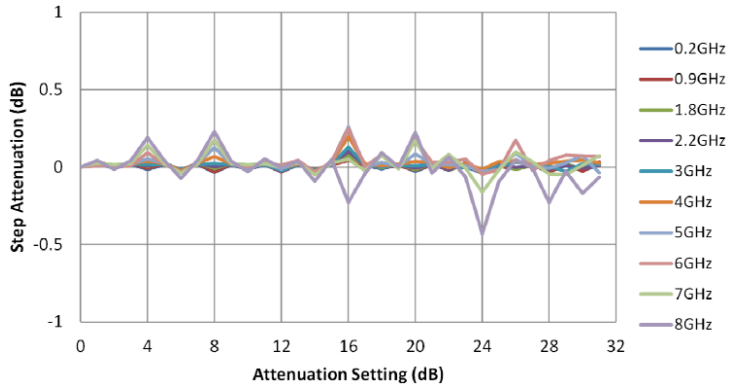



*Figure 13. 1-dB step attenuation vs. frequency(*)*

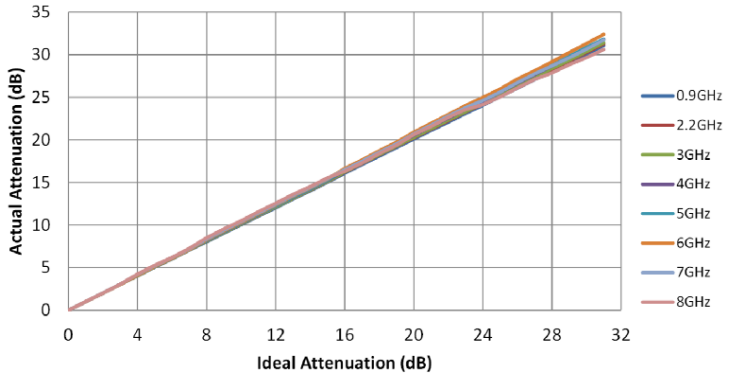



*Figure 14. 1-dB step, actual vs. frequency*

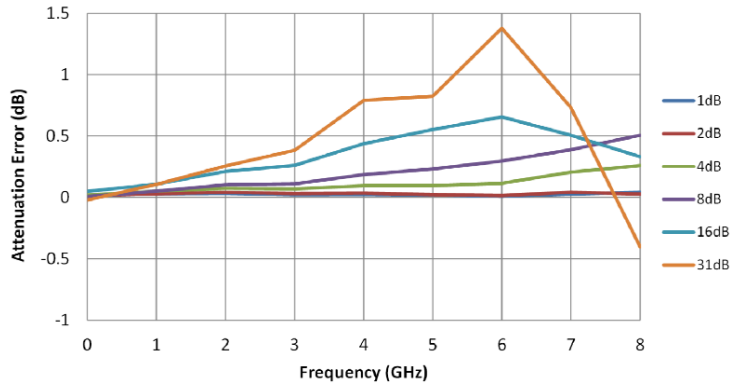



*Figure 15. 1-dB major state bit error vs. attenuation setting*

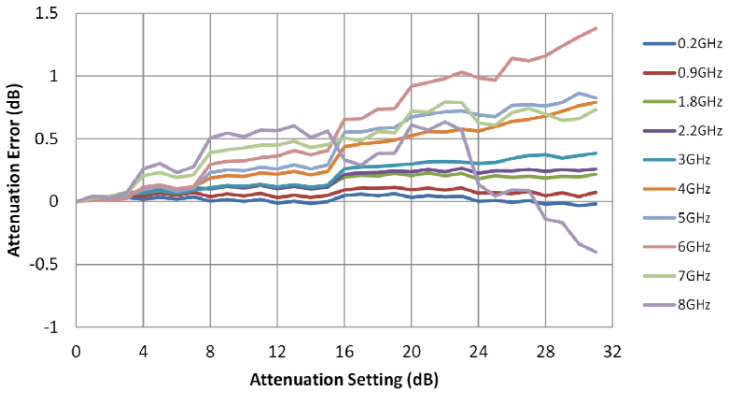



*Figure 16. 1-dB attenuation error vs. frequency*

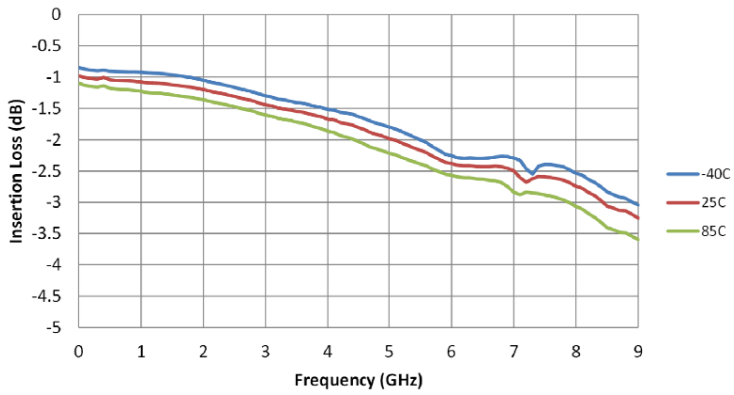



*Figure 17. Insertion loss vs. temperature*

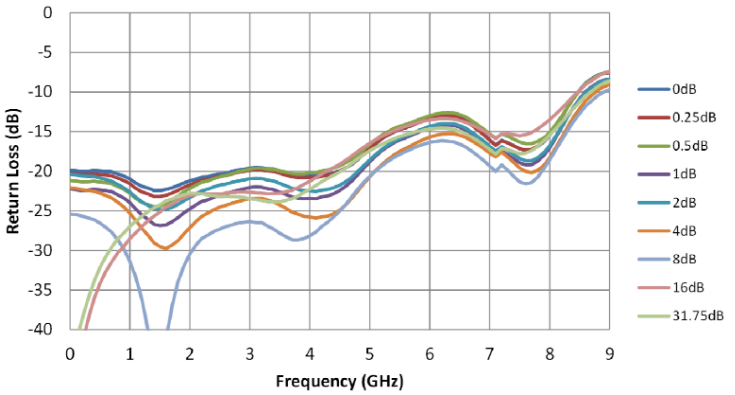



*Figure 18. Input return loss vs. attenuation setting*

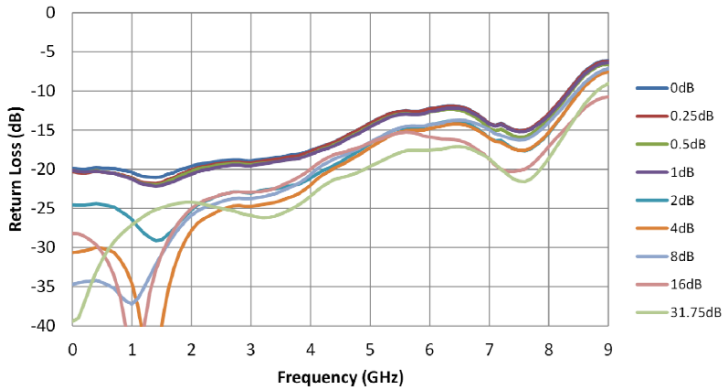



*Figure 19. Output return loss vs. attenuation setting*

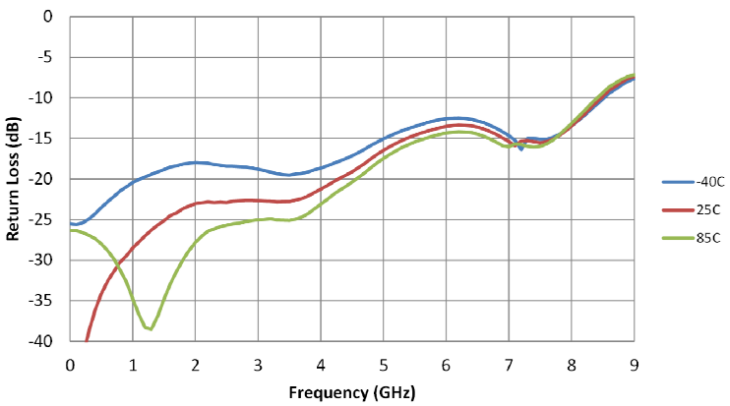



*Figure 20. Input return loss vs. temperature for 16 dB attenuation setting*

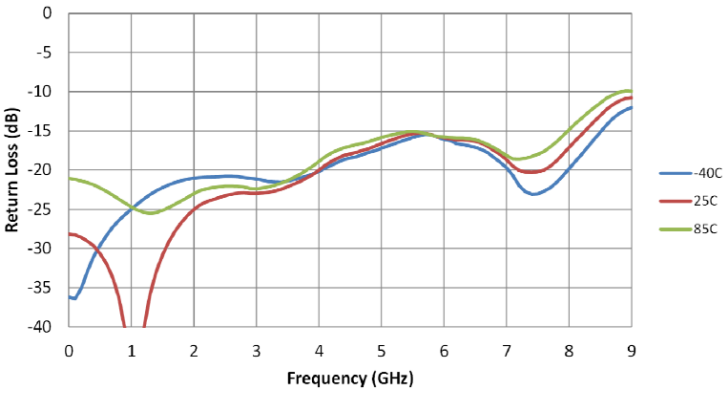



*Figure 21. Output return loss vs. temperature for 16 dB attenuation setting*

* Monotonicity is held as long as the step-attenuation does not cross below –1.0 dB.

Figure 22–Figure 27 show the typical performance data at +25 °C and $V_{DD}$ = 3.4V, unless otherwise specified.

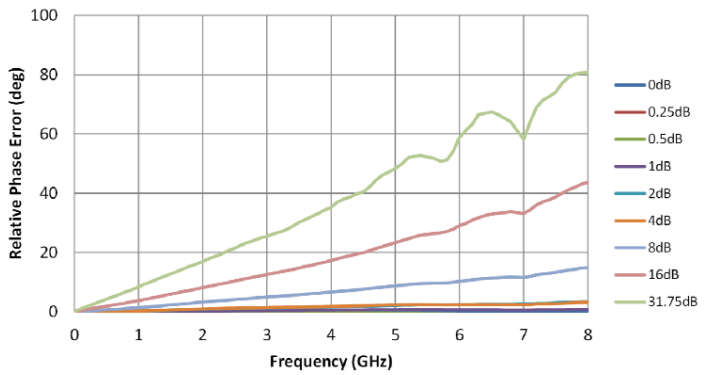



*Figure 22. Relative phase error vs. attenuation setting*

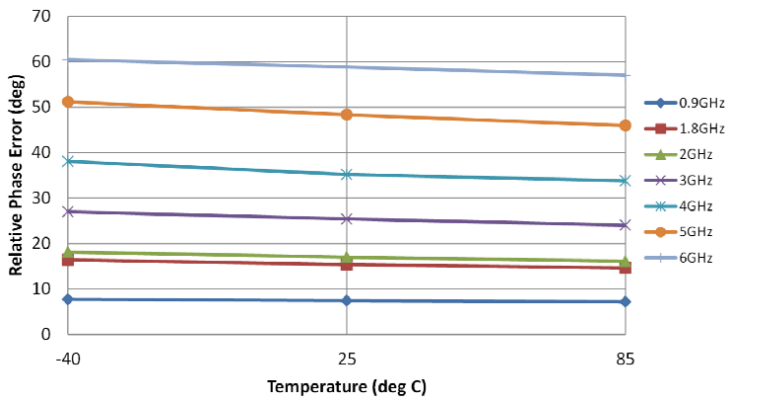



*Figure 23. Relative phase error for 31.75 dB attenuation setting vs. frequency*

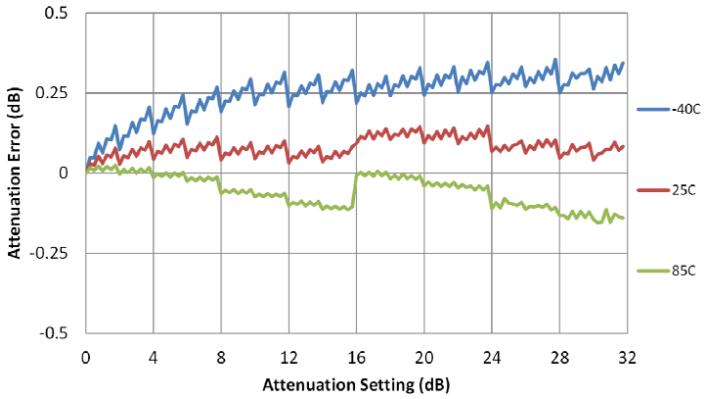



*Figure 24. Attenuation error at 900 MHz vs. temperature*

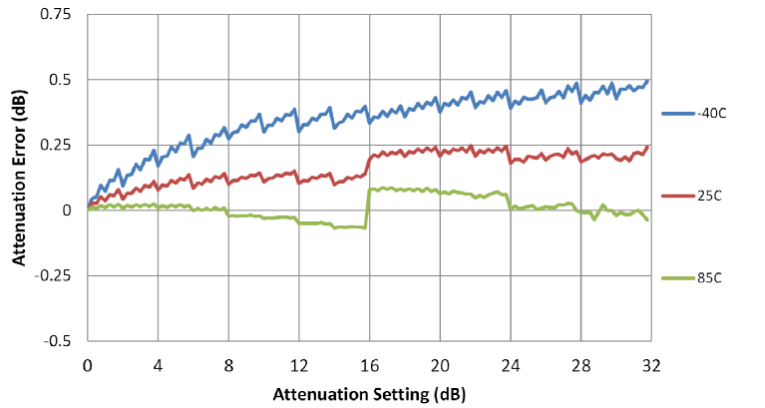



*Figure 25. Attenuation error at 1800 MHz vs. temperature*

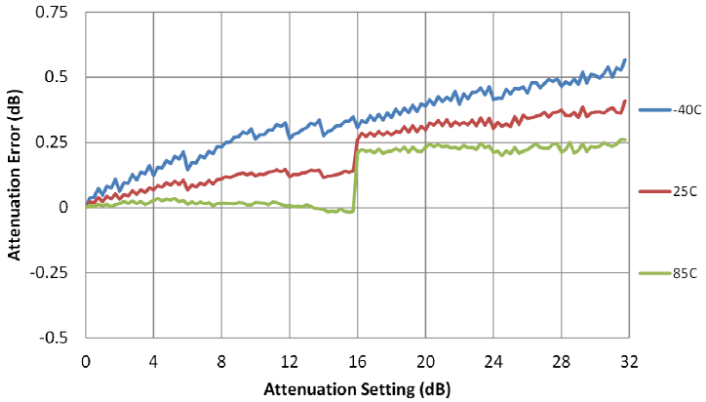



*Figure 26. Attenuation error at 3000 MHz vs. temperature*

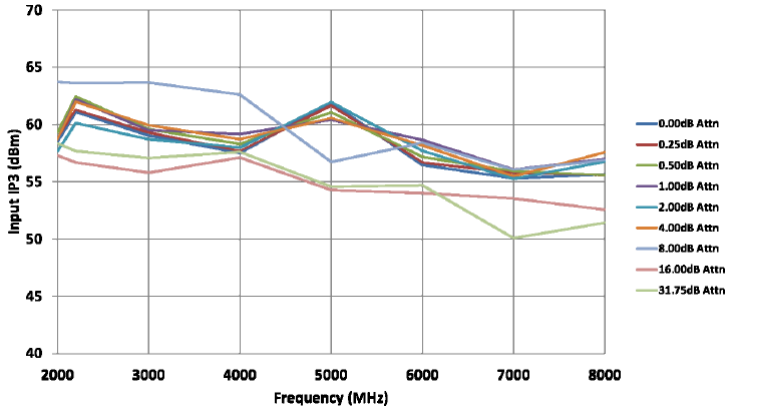



*Figure 27. IIP3 vs. attenuation setting*

# Evaluation kit

pSemi designed the evaluation board (EVB) to ease your evaluation of the PE43704 DSA. The PE43704 EVB supports direct-parallel, latched-parallel, and serial modes.

## Evaluation kit setup

Connect the EVB with the USB dongle board and USB cable as shown in Figure 28.

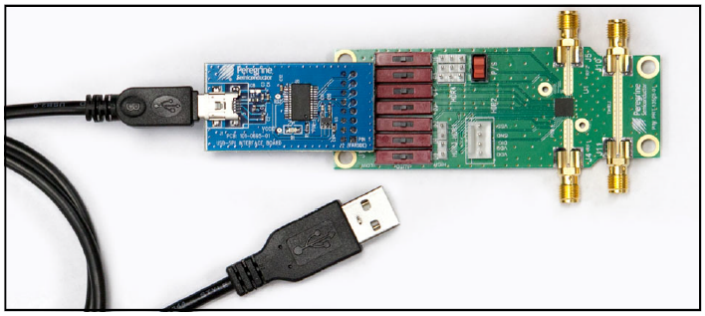


*Figure 28. Evaluation kit*

## Direct-parallel programming procedure

Direct-parallel programming is suitable for manual operation without software programming. For manual direct-parallel programming, position the parallel/serial (P/S) select switch to the parallel (or left) position. The LE pin of J1 (pin 15) must be tied to HIGH voltage. Switches D0–D6 are SP3T switches that you can use to manually program the parallel bits. When D0–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting D0–D6 to the AUTO position presents as OPEN, which is set for software programming of latched-parallel and serial mode. Table 7 lists the parallel programming truth table.

## Latched-parallel programming procedure

For automated latched-parallel programming, connect the USB dongle board and cable provided with the evaluation kit (EVK) from the USB port of the PC to the J1 header of the PE43704 EVB, and set the D0–D6 SP3T switches to the AUTO position. Position the parallel/serial (P/S) select switch to the parallel (or left) position. The evaluation software is written to operate the DSA in parallel mode. Verify that the software GUI is set to latched-parallel mode. Use the software GUI to enable the preferred attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

## Serial-addressable programming procedure

For automated serial programming, connect the USB dongle board and cable provided with the evaluation kit (EVK) from the USB port of the PC to the J1 header of the PE43704 EVB, and set the D0–D6 SP3T switches to the AUTO toggle position. Set the parallel/serial (P/S) select switch to the serial (or right) position. Before programming, define an address setting using the HDR4 header pin:

- Jump the middle row of pins on the HDR4 header (A0–A2) to the lower row of pins to set logic low, or
- Jump the middle row of pins to the upper row of pins to set logic high.

If the HDR4 pins are left open, the default address is 000. The software GUI is written to operate the DSA in serial mode. Use the software GUI to enable each setting to the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

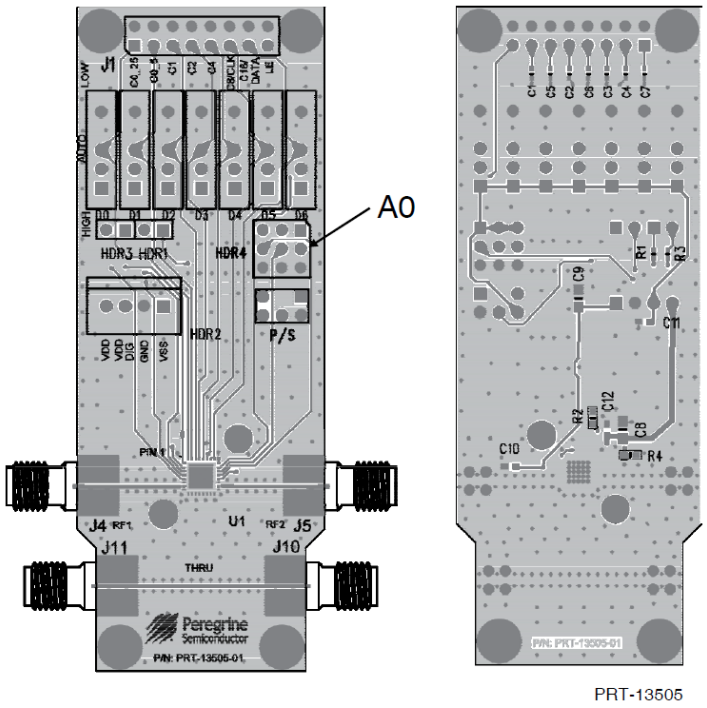



*Figure 29. Evaluation board layout*

# Evaluation board schematic

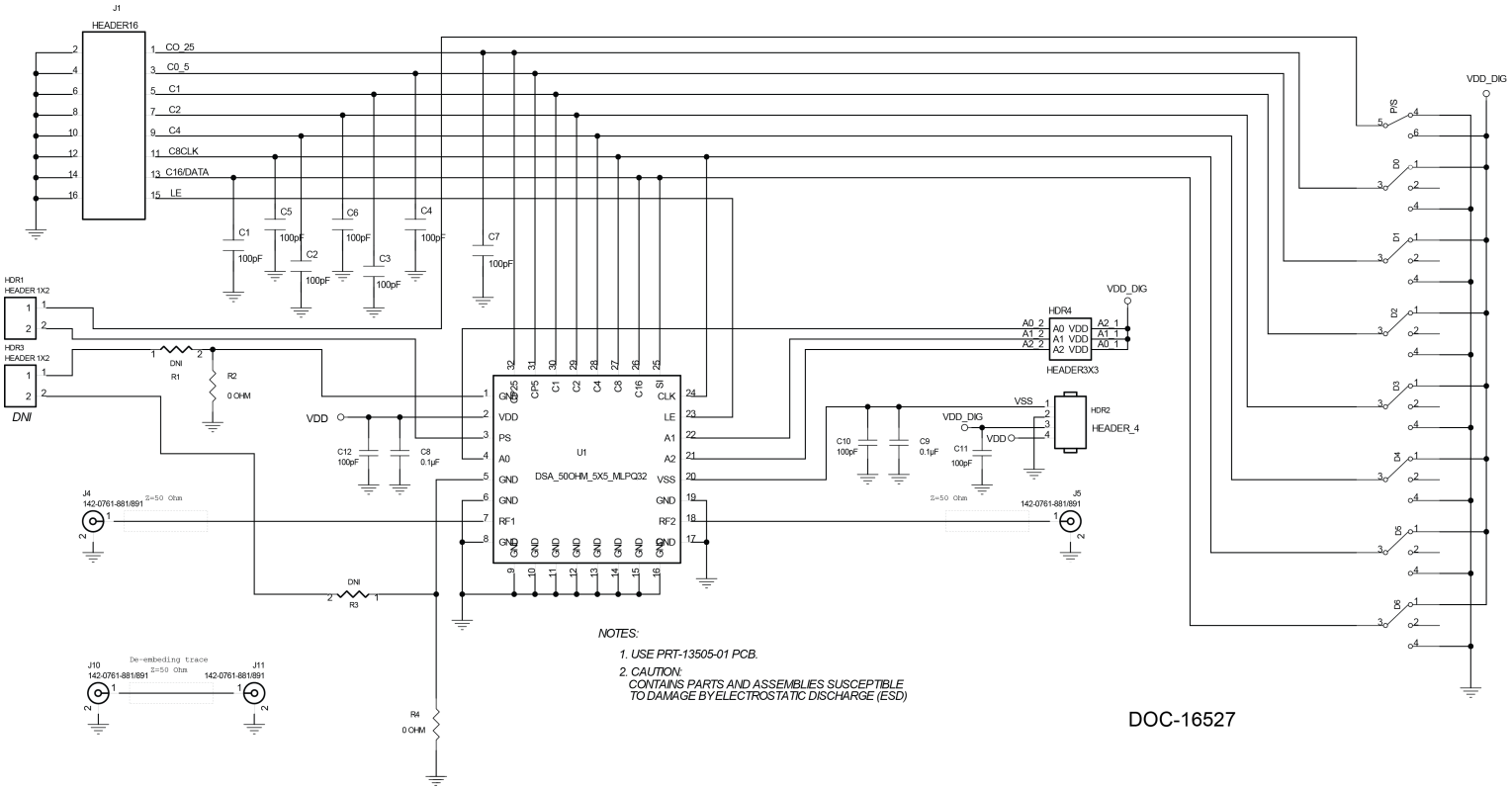



*Figure 30. Evaluation board schematic*

# Pin information

Figure 31 shows the PE43704 pin map for the 32-lead 5×5 QFN package, and Table 13 lists the description for each pin.

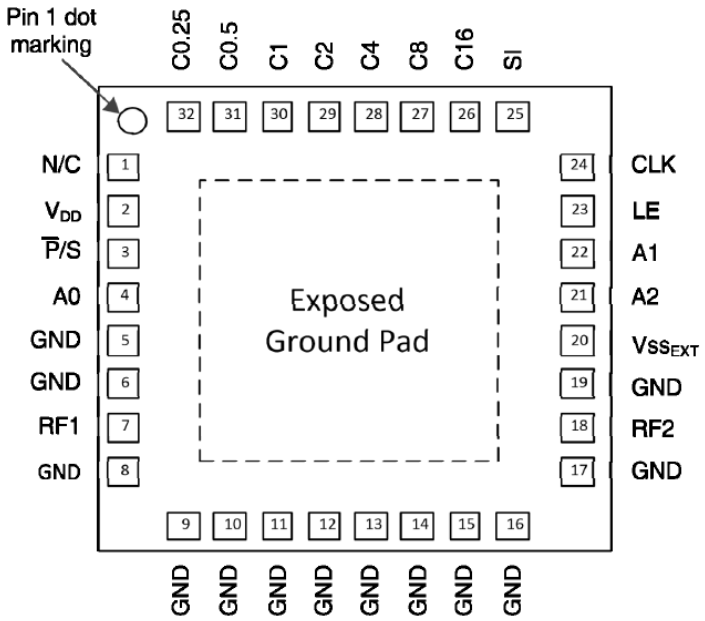



*Figure 31. Pin configuration (top view)*

1. RF pins 7 and 18 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use $Vss_{EXT}$ (pin 20) to bypass and disable internal the negative voltage generator. Connect $Vss_{EXT}$ (pin 20) to GND ($Vss_{EXT}$ = 0V) to enable the internal negative voltage generator.
3. Ground C16, C8, C4, C2, C1, C0.5, and C0.25 (pins 26–32) if not in use.

Table 13. PE43704 pin descriptions

| Pin no. | Pin name | Description |
|---|---|---|
| 1 | N/C | No connect |
| 2 | $V_{DD}$ | Supply voltage |
| 3 | P/S | Serial/parallel mode select |
| 4 | A0 | Address bit 0 connection |
| 5, 6, 8–17, 19 | GND | Ground |
| 7[1] | RF1 | RF1 port (RF input) |
| 18[1] | RF2 | RF2 port (RF output) |
| 20[2] | $Vss_{EXT}$ | External Vss negative voltage control |
| 21 | A2 | Address bit A2 connection |
| 22 | A1 | Address bit A1 connection |
| 23 | LE | Serial interface latch enable input |
| 24 | CLK | Serial interface clock input |
| 25 | SI | Serial interface data input |
| 26[3] | C16 (D6) | Parallel control bit, 16 dB |
| 27[3] | C8 (D5) | Parallel control bit, 8 dB |
| 28[3] | C4 (D4) | Parallel control bit, 4 dB |
| 29[3] | C2 (D3) | Parallel control bit, 2 dB |
| 30[3] | C1 (D2) | Parallel control bit, 1 dB |
| 31[3] | C0.5 (D1) | Parallel control bit, 0.5 dB |
| 32[3] | C0.25 (D0) | Parallel control bit, 0.25 dB |
| Pad | GND | Exposed pad. Ground for proper operation. |

# Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

## Moisture sensitivity level

The PE43704 moisture sensitivity level rating for the 32-lead 5×5 QFN package is MSL1.

## Package drawing

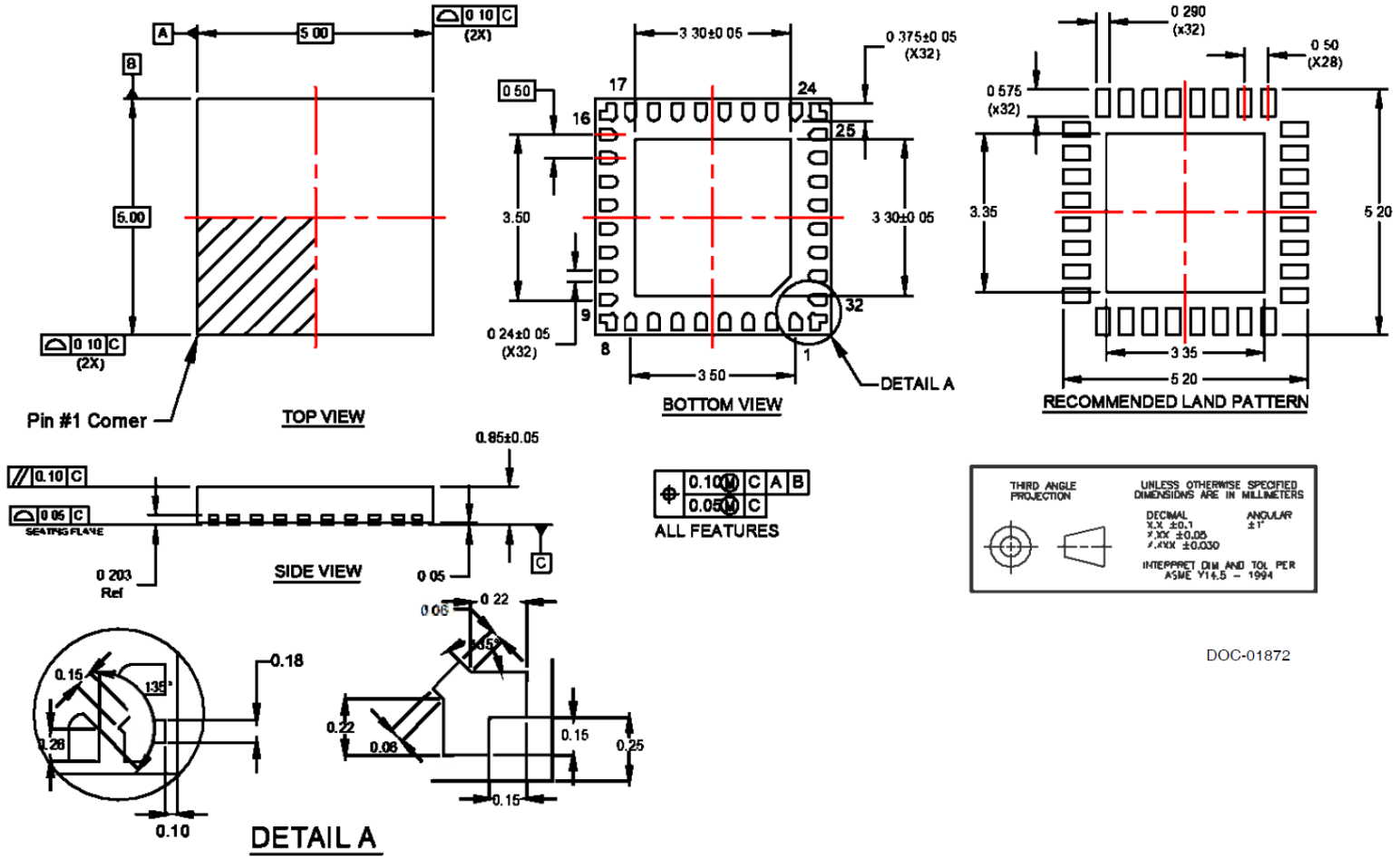



*Figure 32. Package mechanical drawing for the 32-lead 5×5 QFN package*

## Top-marking specification


● = Pin 1 designator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZZ = Assembly lot code (maximum seven characters)

*Figure 33. PE43704 package marking specification*

## Tape and reel specification

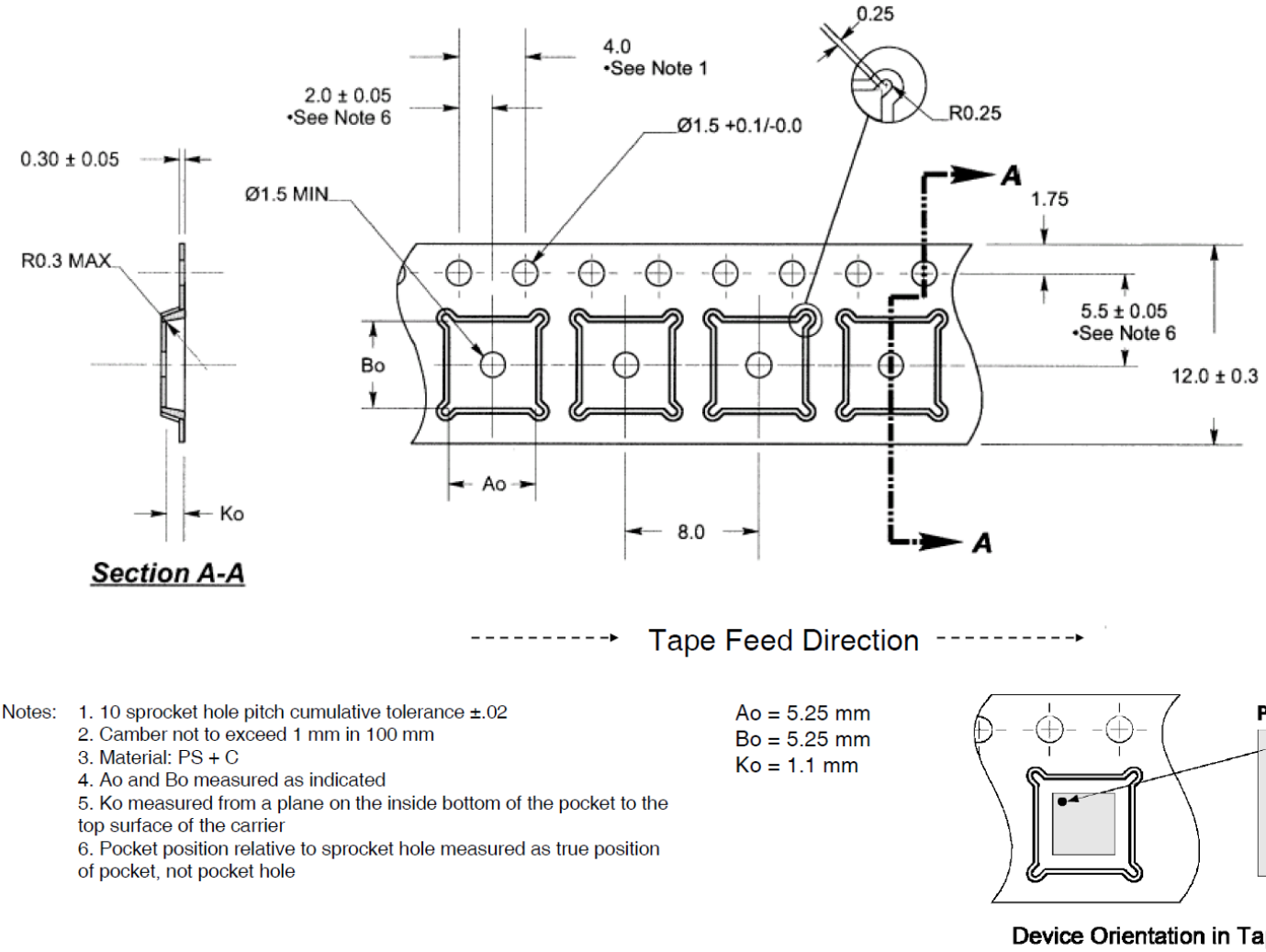



*Figure 34. Tape and reel specification for the 32-lead 5×5 QFN package*

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

# Ordering information

| Order code | Description | Packaging | Shipping method |
|---|---|---|---|
| PE43704B-Z | PE43704 digital step attenuator | 32-lead 5×5 QFN | 3000 units/T&R |
| EK43704-12 | PE43704 evaluation kit | Evaluation kit | 1/box |

# Document categories

| | |
|---|---|
| **Advance Information** | The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice. |
| **Preliminary Specification** | The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product. |
| **Product Specification** | The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF). |
| **Product Brief** | This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com. |

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