PE45450

Document category: Product Specification

UltraCMOS® Power Limiter, 9 kHz–6 GHz

Features

- Monolithic drop-in solution with no external bias components, reducing design complexity
- Adjustable power limiting threshold from +25 dBm to +35 dBm
- Maximum power handling:
  - +40 dBm CW (10W)
  - +47 dBm pulsed (50W)
- Superior ESD rating and protection:
  - 8 kV HBM on all pins
  - 1 kV CDM on all pins
  - 600V MM on all pins
- Unbiased power limiting operation
- Fast response and recovery time of 1 ns
- Dual mode operation:
  - Power limiting mode
  - Power reflecting mode
- Packaging: 12-lead 3 × 3 mm QFN

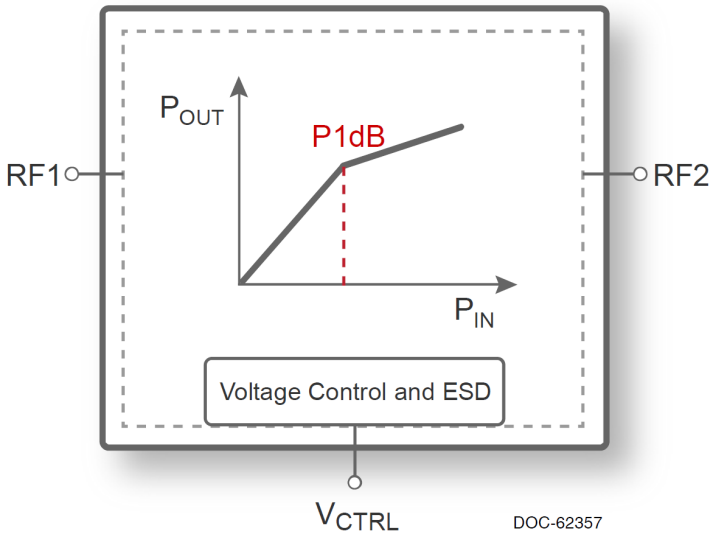

Figure 1. PE45450 functional diagram

Product description

The PE45450 is a HaRP™ technology-enhanced power limiter designed for use in high-performance power limiting applications in test and measurement equipment, radar, military electronic countermeasure receivers, and wireless infrastructure transceivers and antennas.

Unlike traditional PIN diode solutions, the PE45450 achieves an adjustable input 1-dB compression point or limiting threshold via a low current control voltage (V_{CTRL}), eliminating the need for external bias components, such as DC blocking capacitors, RF choke inductors, and bias resistors.

The PE45450 delivers low insertion loss and high linearity under non-limiting input power levels and extremely fast response and recovery time in a limiting event. It also offers a superior ESD rating and protection for subsequent circuitry.

The PE45450 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE45450 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Control voltage: - Power limiting mode - Power reflecting mode	V_{CTRL}	-3.3	3.6	V
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM, all pins(1)	$V_{ESD,HBM}$	–	8000	V
ESD voltage MM, all pins(2)	$V_{ESD,MM}$	–	600	V
ESD voltage CDM, all pins(3)	$V_{ESD,CDM}$	–	1000	V

1. Human Body Model (HBM, MIL_STD 883 Method 3015.7).
2. Machine Model (JEDEC JESD22-A115).
3. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE45450 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE45450 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Control voltage: - Power limiting mode - Power reflecting mode	V_{CTRL}	 -2.5 -2.5	–	 -0.5 +2.5	V
RF input power, CW(1)	$P_{MAX,CW}$	–	–	40	dBm
RF input power, pulsed(2)	$P_{MAX,PULSED}$	–	–	47	dBm
RF input power, unbiased(3)	$P_{MAX,UNB}$	–	–	47	dBm
Operating temperature range	T_{OP}	-55	+25	+85	°C
Operating junction temperature	T_J	–	–	+290	°C

1. CW, 100% duty cycle, in 10 min, 50Ω.
2. Pulsed, 0.1% duty cycle of 1-µs pulse width in 10 min, 50Ω.
3. V_{CTRL} = 0V or V_{CTRL} pin left not connected.

Electrical specifications

Table 3 lists the PE45450 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE45450 electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency	–	9 kHz	–	6 GHz	As shown
Power limiting mode					
Insertion loss(1)	9 kHz–3 GHz 3–6 GHz	–	0.45 0.80	0.70 1.05	dB
Return loss(1)	9 kHz–3 GHz 3–6 GHz	–	13 17	–	dB
P1dB/limiting threshold	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –1.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz	–	35 32 25	–	dBm
Leakage power(2)	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –1.5V @ 915 MHz V_{CTRL} = –0.5V @ 915 MHz	–	33.5 33 31.5	35.5 35 33.5	dBm
Leakage power slope	V_{CTRL} = –1.0V @ 915 MHz	–	0.4	–	dB/dB
Unbiased leakage power(2)	V_{CTRL} = 0V @ 915 MHz	–	25	27	dBm
Input IP2	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –2.5V @ 6 GHz	–	115 110	–	dBm
Input IP3	V_{CTRL} = –2.5V @ 915 MHz V_{CTRL} = –2.5V @ 6 GHz	–	70 60	–	dBm
Response/recovery time	1 GHz	–	1	–	ns
Power reflecting mode(3)					
Leakage power(2)	V_{CTRL} = –2.5V @ 915 MHz	–	2	8	dBm
Switching time(4)	State change to 10% RF	–	400	–	µs

1. External matching is required to achieve the performance.
2. Measured with +40 dBm CW applied at input.
3. This mode requires the control voltage to toggle between +2.5V and –2.5V. At +2.5V, the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source.
4. State change is V_{CTRL} toggle from –2.5V to +2.5V.

ESD protection capability

The PE45450 can be used as an ESD protection device to protect sensitive circuit elements against ESD surges. Besides its superior ESD rating of 8 kV HBM, the PE45450 has an excellent voltage clamping capability. During an ESD event, the PE45450 maintains an extremely low voltage across the device to ensure that the circuit element it is protecting survives.

Table 4. Transmission line pulse data vs. HBM

V_{CTRL}	HBM (V)	Max current (A)	Voltage (V)
0	1000	0.7	3.7
-1.5	1000	0.7	18
0	2000	1.3	7
-1.5	2000	1.3	20
0	3000	2.0	10.8
-1.5	3000	2.0	21.5

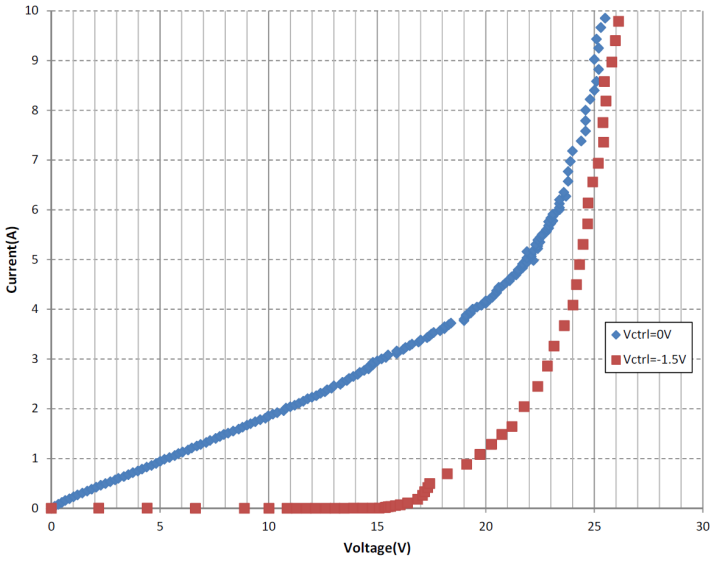


Figure 2. Transmission line pulse curve

Dual mode operation

Power limiting mode

The PE45450 performs as a linear power limiter with an adjustable P1dB/limiting threshold. Adjust the P1dB/limiting threshold by changing the control voltage between –2.5V and –0.5V. If unbiased, or if V_{CTRL} = 0V, the PE45450 still offers power limiting protection.

Power reflecting mode

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +2.5V and –2.5V based on the system protection requirements. At +2.5V, the limiter impedance to ground is less than 1Ω and most of the incident power is reflected back to the source. At –2.5V, the device operates in power limiting mode.

Thermal data

When limiting high-power RF signals, the junction temperature of the power limiter can rise significantly.

The PCB design must properly dissipate the heat away from the part and maintain the 290 °C peak junction temperature.

Use best design practices for high-power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Prevent solder from voiding under the part.

Table 5. Theta JC

Parameter	Min	Typ	Max	Unit
Theta JC	–	20	–	°C/W

Typical performance data

Figure 3–Figure 13 show the typical performance data at +25 °C and 915 MHz (Z_S = Z_L = 50Ω), unless otherwise specified.

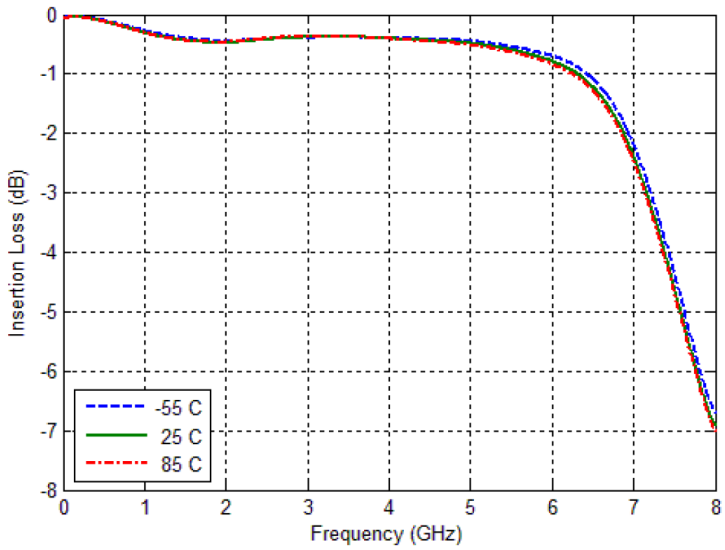


Figure 3. Insertion loss vs. temperature

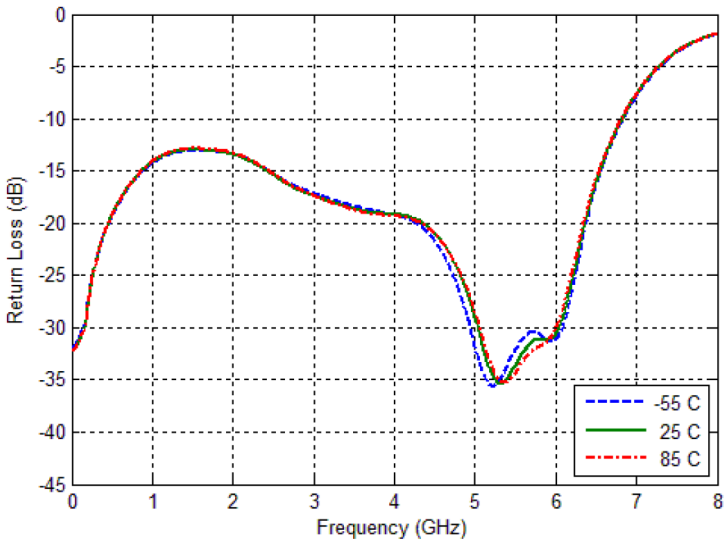


Figure 4. Input return loss vs. temperature

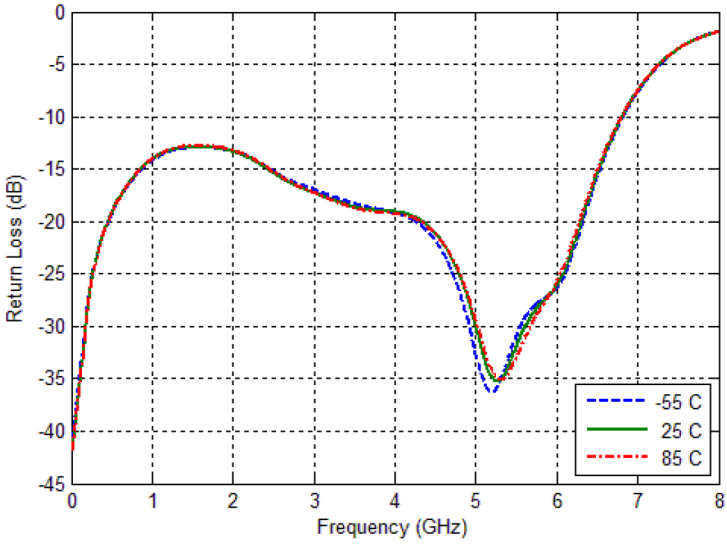


Figure 5. Output return loss vs. temperature

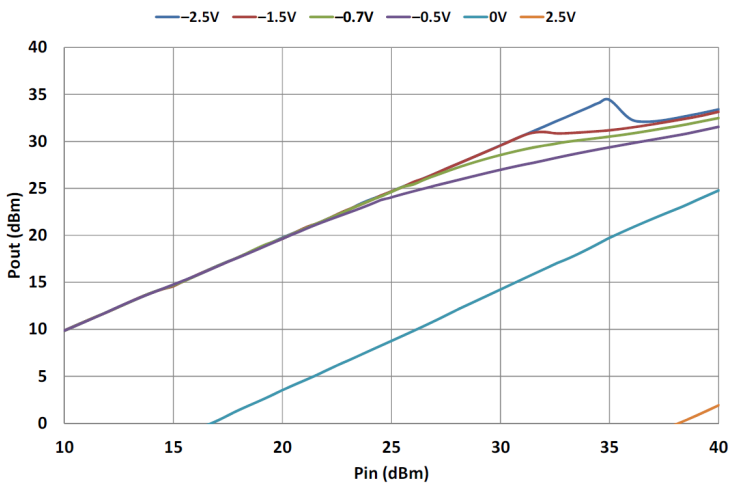


Figure 6. P_{OUT} vs P_{IN} over V_{CTRL}

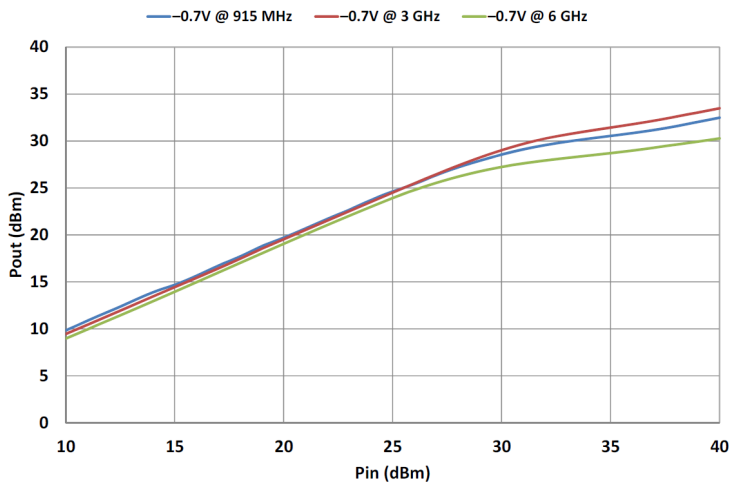


Figure 7. P_{OUT} vs P_{IN} over frequency @ V_{CTRL} = -0.7V

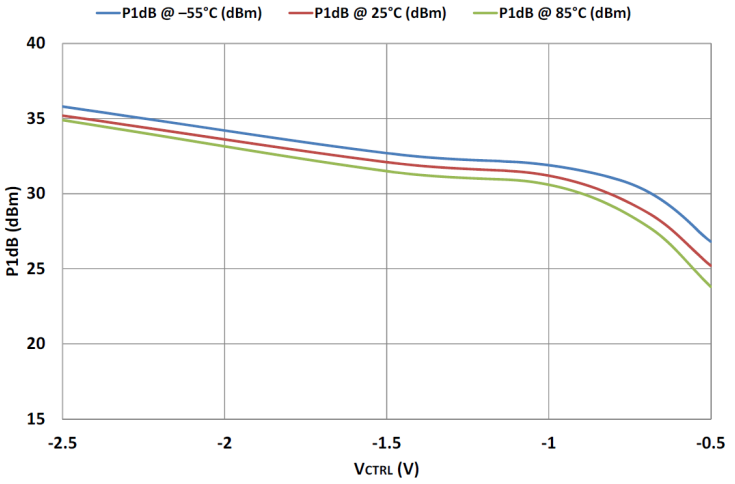


Figure 8. P1dB vs. V_{CTRL} over temperature

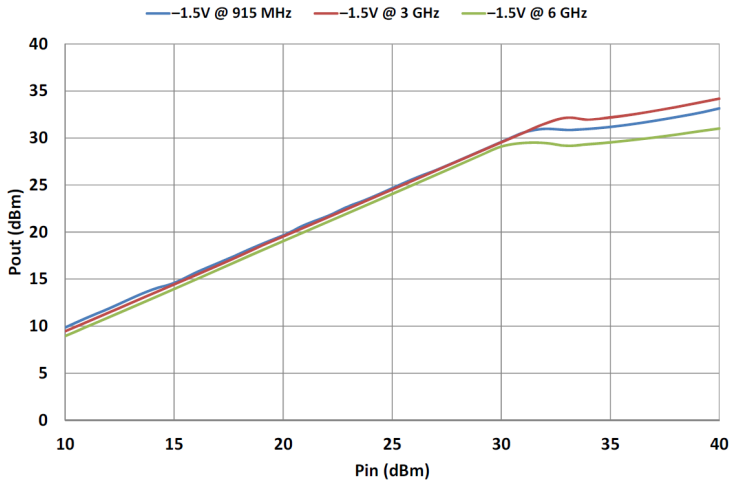


Figure 9. P_{OUT} vs P_{IN} over frequency @ V_{CTRL} = -1.5V

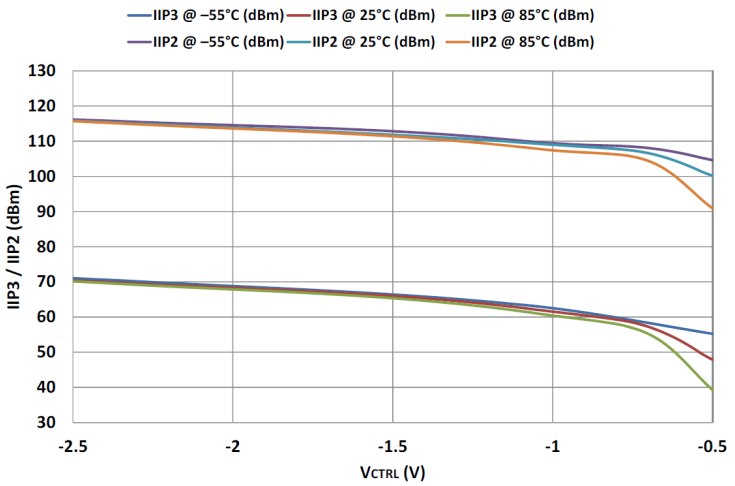


Figure 10. IIP3/IIP2 vs. V_{CTRL} over temperature

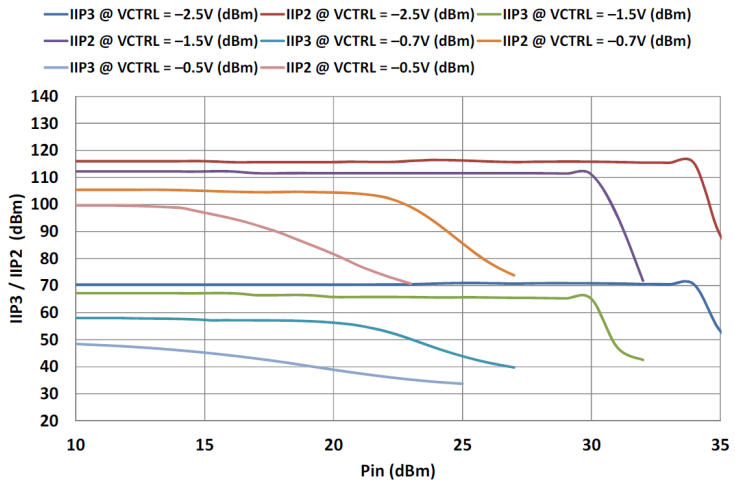


Figure 11. IIP3/IIP2 vs. P_{IN} over V_{CTRL}

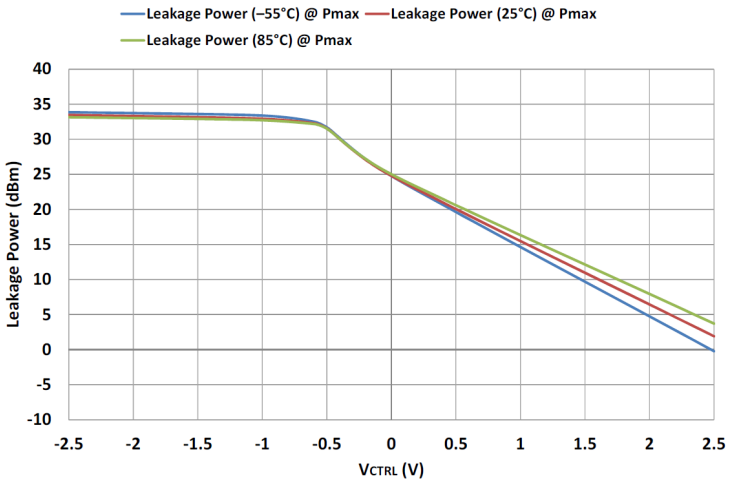


Figure 12. Leakage power @ P_{MAX} vs. V_{CTRL} over temperature

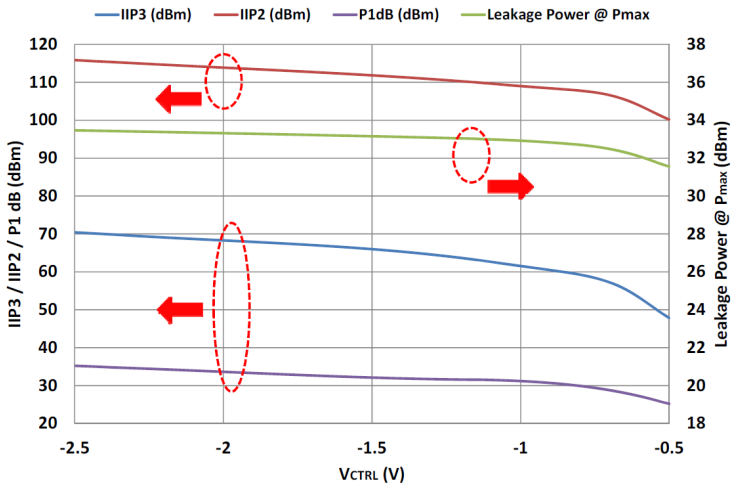


Figure 13. P1dB, IIP3, IIP2, leakage power @ P_{MAX} vs. V_{CTRL}

Evaluation kit

pSemi designed the power limiter EVK board to ease your evaluation of the pSemi PE45450. The bidirectional RF input and output connect to RF1 and RF2 port through a 50Ω transmission line via SMA connectors J2 and J3. A through 50Ω transmission line is available via SMA connectors J5 and J6. You can use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connector J4 connects to the external bias V_{CTRL}.

The board is constructed of a 4-metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and Er = 3.66. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

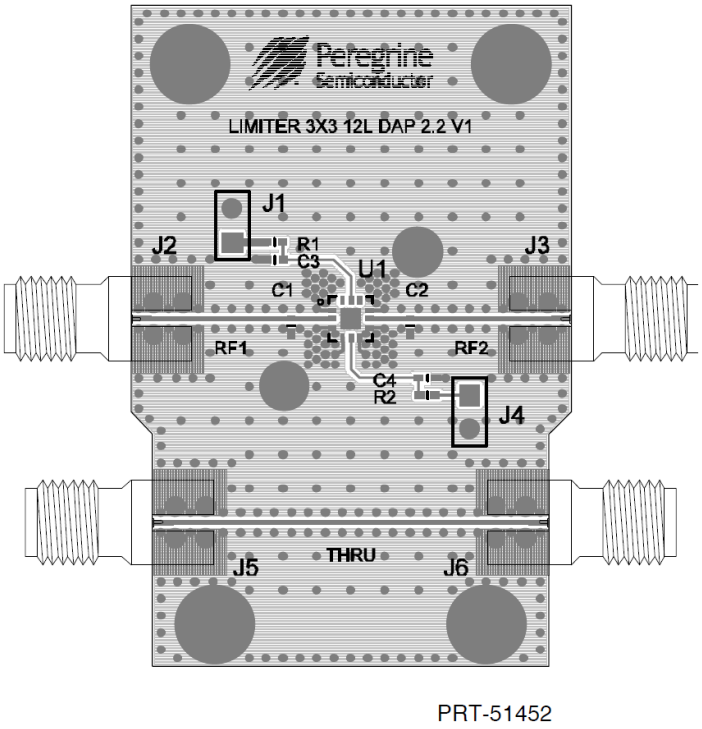
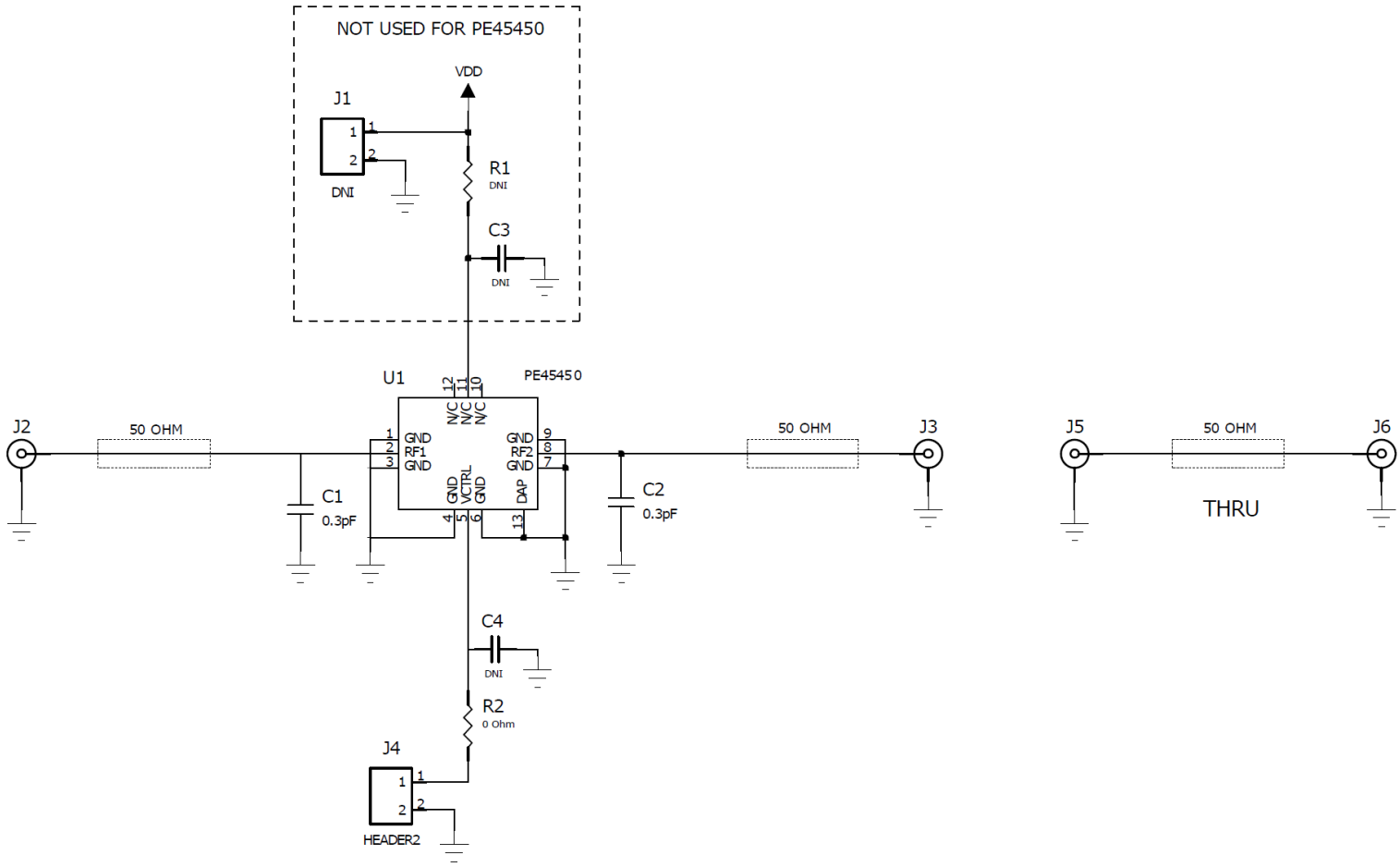


Figure 14. Evaluation board layout

Evaluation board schematic



Caution: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

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Figure 15. Evaluation board schematic

Pin information

Figure 16 shows the PE45450 pin map for the 12-lead 3 × 3 mm QFN package, and Table 6 lists the description for each pin.

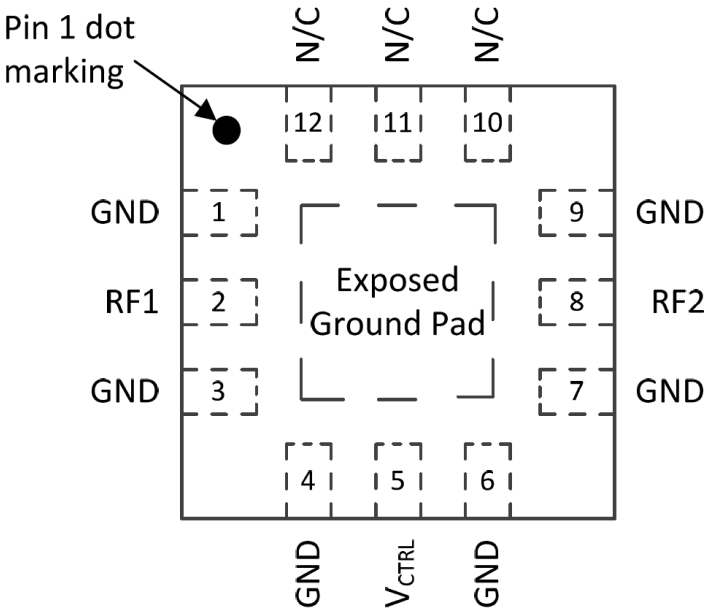


Figure 16. Pin configuration (top view)

Table 6. PE45450 pin descriptions

Pin no.	Pin name	Description
1, 3, 4, 6, 7, 9	GND	Ground
2[1]	RF1	RF port 1
5	V_{CTRL}	Control voltage
8[1]	RF2	RF port 2
10–12[2]	N/C	No connect
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 2 and 8 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pins 10–12 can be ground if needed.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE45450 moisture sensitivity level rating for the 12-lead 3 × 3 mm QFN package is MSL1.

Package drawing

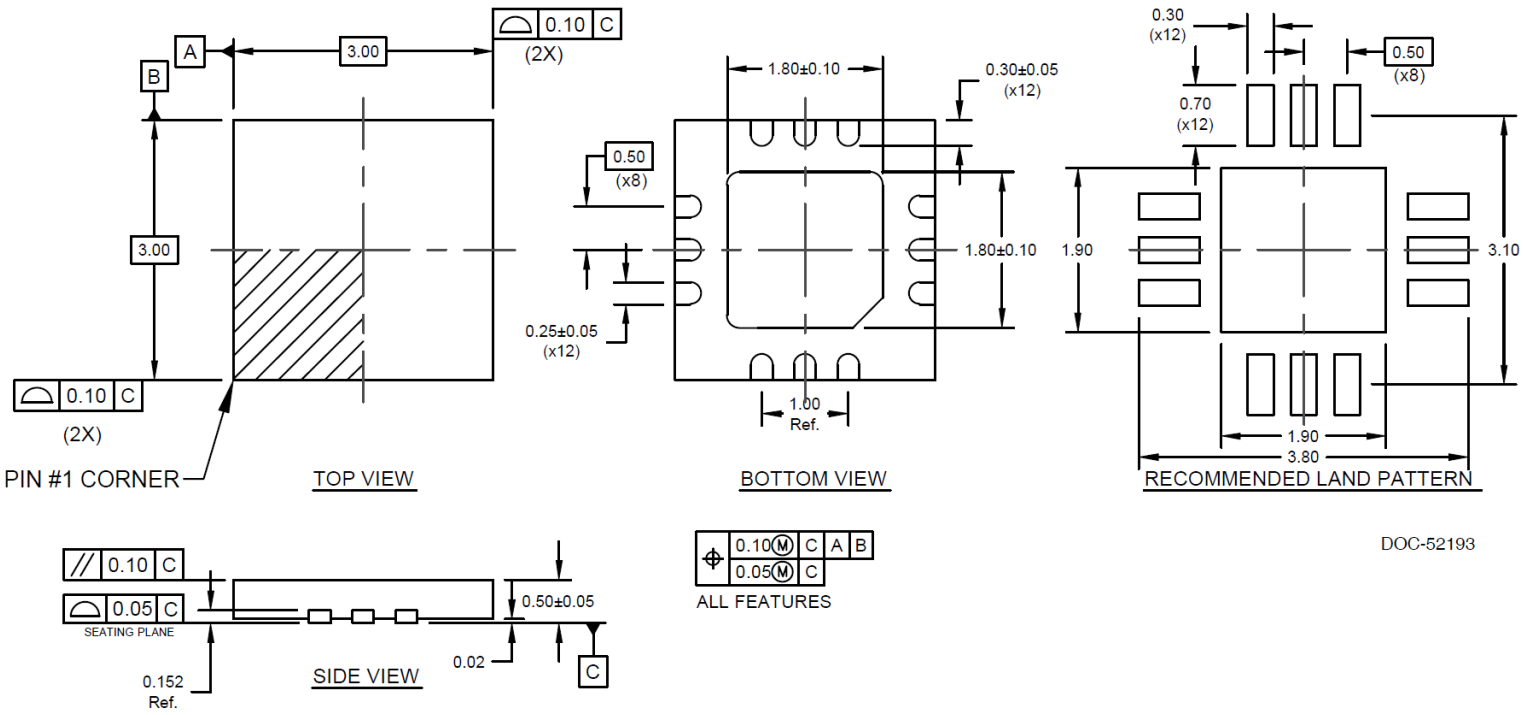


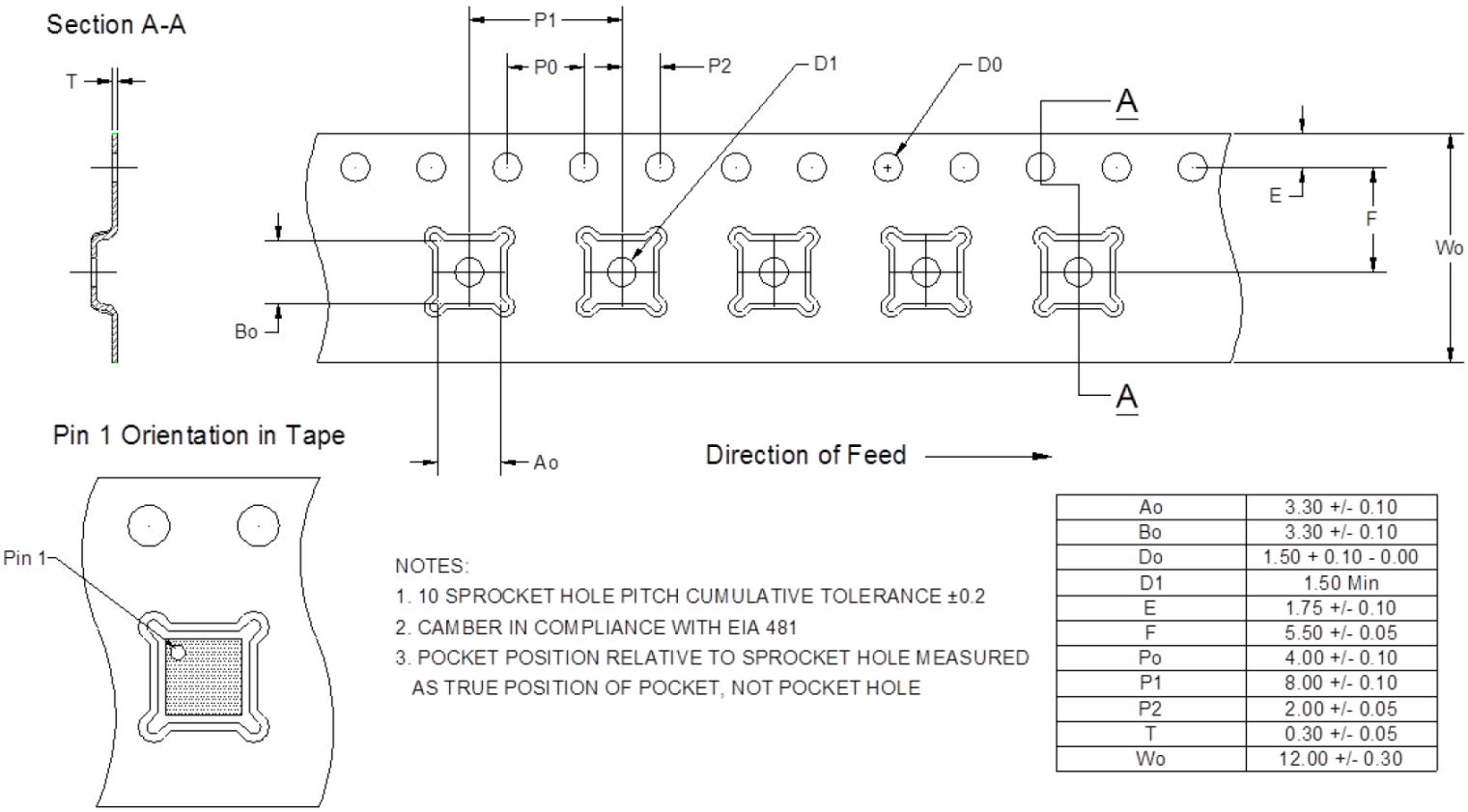
Figure 17. Package mechanical drawing for the 12-lead 3 × 3 mm QFN package

Top-marking specification

● = Pin 1 designator
45450 = Five digit part number
YYWW = Date Code, last two digits of the year and work week
ZZZZZZ = Maximum six characters of the assembly lot code

Figure 18. PE45450 package marking specification

Tape and reel specification



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

Ao	3.30 +/- 0.10
Bo	3.30 +/- 0.10
Do	1.50 + 0.10 - 0.00
D1	1.50 Min
E	1.75 +/- 0.10
F	5.50 +/- 0.05
Po	4.00 +/- 0.10
P1	8.00 +/- 0.10
P2	2.00 +/- 0.05
T	0.30 +/- 0.05
Wo	12.00 +/- 0.30

Figure 19. Tape and reel specification for the 12-lead 3 × 3 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE45450A-X	PE45450 power limiter	Green 12-lead 3 × 3 mm QFN	500 units/T&R
EK45450-02	PE45450 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
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