PE42545 Performance Optimization

Application Note 102

Summary

This application note provides the recommended land pattern and assembly process for achieving optimum performance with the PE42545. The PE42545 is a flip-chip, single-pole four-throw (SP4T) switch that supports a wide frequency range from 9 kHz to 67 GHz. The PE42545 is suited for test and measurement (T&M), microwave back-haul, and radar applications.

Introduction

The PE42545 is a HaRP™ technology-enhanced reflective SP4T RF switch die that supports a wide frequency range from 9 kHz to 67 GHz. It delivers low insertion loss, fast switching time and high isolation performance, making this device ideal for test and measurement (T&M), 5G mmWave, microwave backhaul, radar and satellite communication applications, achieving 3.2 dB of insertion loss and greater than 28 dB of isolation @ 60 GHz. The PE42545 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology.

Product Overview

The PE42545 is a flip-chip SP4T switch utilizing lead-free solder ball technology to provide the signal and ground interconnect. Solder reflow profiles common to lead-free surface-mount device (SMD) assembly can be readily used to achieve uniform and reliable attachment.

Bump Information

Figure 1 shows the bump map for the PE42545. All unlabeled bumps are GND. Table 1 provides detailed bump descriptions. To ease routing and manufacturing, the bump configuration maintains a minimum of 500 µm (0.5 mm) pitch between all unique signal pads.

Figure 1 ▪ Bump Configuration (Bumps Up)

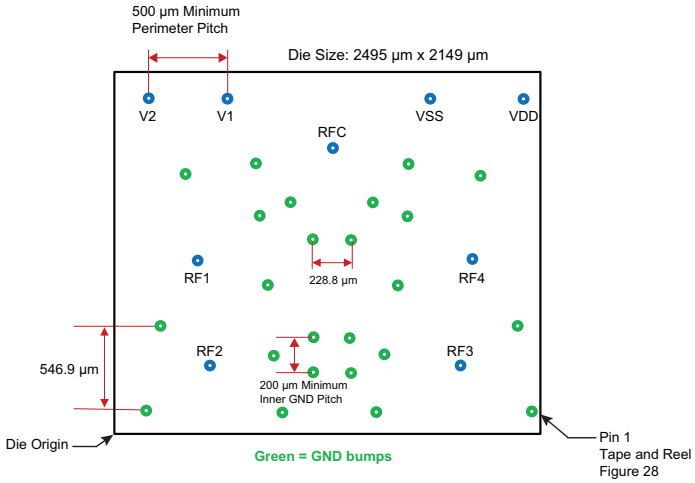


Table 1 ▪ Bump Descriptions for PE42545

Bump Name	Description
GND	Ground
RF1	RF throw port 1
RF2	RF throw port 2
RF3	RF throw port 3
RF4	RF throw port 4
RFC	RF common port
V1	Control input 1
V2	Control input 2
VDD	Positive supply voltage
VSS	Negative supply voltage

Table 2 ▪ Bump Coordinates for PE42545

Bump No.	Bump Name	Description	From Die Origin (µm)(*)	
			X	Y
1	V2	Control input 2	128.5	1960.5
2	V1	Control input 1	628.5	1960.5
3	VSS	Negative supply voltage	1811.5	1960.5
4	VDD	Positive supply voltage	2311.5	1960.5
5	GND	Ground	2348.5	88.5
6	GND	Ground	1523.5	106.615
7	GND	Ground	916.5	106.615
8	GND	Ground	91.5	88.5
9	GND	Ground	128.5	635.405
10	GND	Ground	361.385	1516.71
11	RF1	RF throw port 1	434.5	1020.38
12	RF2	RF throw port 2	488.505	398.51
13	GND	Ground	791.5	1263.5
14	GND	Ground	774.13	1577.87
15	GND	Ground	866.5	461.615
16	GND	Ground	841.5	866.35
17	GND	Ground	980.58	1353.17
18	GND	Ground	1105.58	366.945
19	GND	Ground	1105.58	566.945
20	GND	Ground	1105.58	1138.17
21	RFC	RF common port	1220	1676
22	GND	Ground	1334.42	366.945
23	GND	Ground	1334.42	566.945
24	GND	Ground	1334.42	1138.17
25	GND	Ground	1459.42	1353.17
26	GND	Ground	1573.5	461.615
27	GND	Ground	1598.5	866.35
28	GND	Ground	1648.5	1263.5

Note: * All bump locations originate from the die origin.

Table 2 ▪ Bump Coordinates for PE42545 (Cont.)

Bump No.	Bump Name	Description	From Die Origin (µm)(*)	
			X	Y
29	GND	Ground	1665.87	1577.87
30	RF3	RF throw port 3	1951.495	398.51
31	RF4	RF throw port 4	2005.5	1020.38
32	GND	Ground	2078.615	1516.71
33	GND	Ground	2311.5	635.405

Note: * All bump locations originate from the die origin.

Land Pattern

The PE42545 is a flip-chip die configured with a 500 µm minimum ball pitch for perimeter IO bumps with 200 µm minimum pitch inner GND bumps. Thin film technologies can readily meet the line width and spacing critical dimensions (CD) of 100 µm or less.

To obtain the best microwave performance, specific metallization and via patterns and solder mask openings have been defined and implemented to provide measured results for the PE42545. These recommended layouts can be downloaded from the pSemi website. Deviations from recommended layouts can result in decreased performance.

Astra® MT77 Printed Circuit Board—High Frequency Probe (PRT-80235)

A metallization and via pattern of PRT80235 has been generated with the ASTRA MT77 substrate. **Figure 2** illustrates the recommended top layer metallization and via placements used when utilizing an RF probe. **Figure 3** details the four-layer PCB stack-up using a 2.5 mil (.0635 mm) Astra MT77 RF core.

Important parameters for the coplanar waveguide with ground (CPWG) transmission lines are as follows:

- RF common port (RFC) transitions from a 50Ω input to a 60Ω line of length 200 µm
- RF1 through RF4 ports transition from 50Ω transmission lines to 68Ω lines of length 450 µm

Figure 2 ▪ PRT-80235 PCB Substrate Metallization and Via Pattern Used for High Frequency Probes

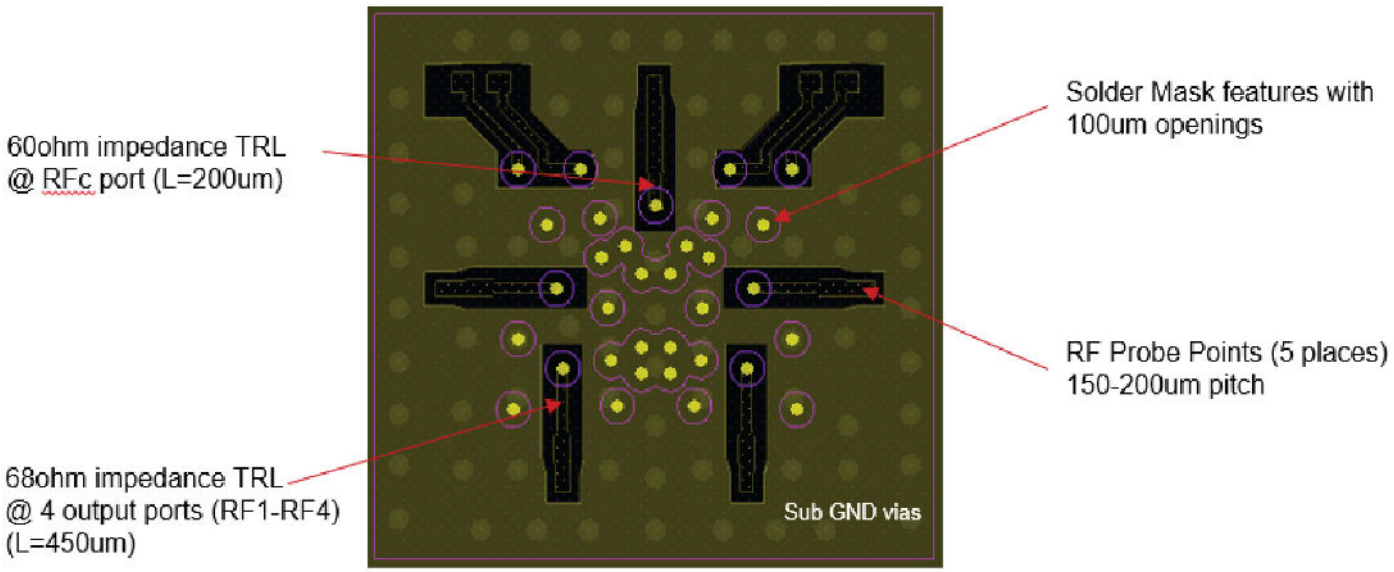
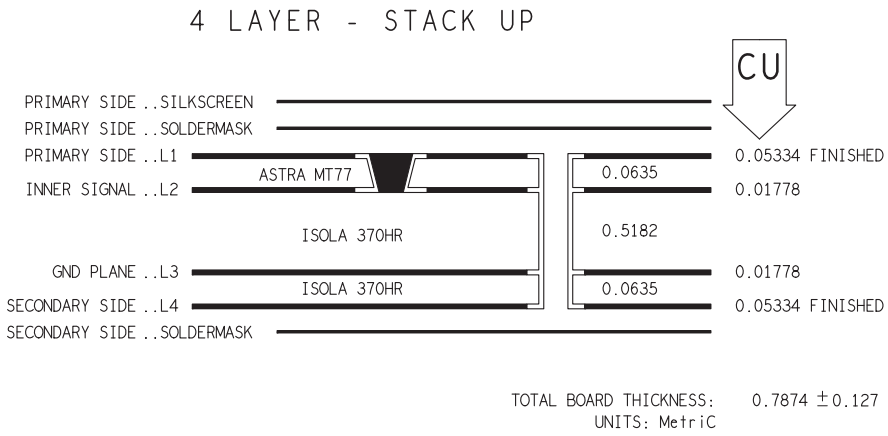


Figure 3 ▪ PRT-80235 Printed Circuit Board Composition



In general, for different RF core dielectrics and thicknesses, the critical dimensions of line width and spacing and via diameter can be readily scaled to accommodate the specific thickness requirements.

Astra Printed MT77 Circuit Board—SMA Connector (PRT-80002)

A metallization and via pattern for PRT80002 has been generated with ASTRA MT77 substrate. **Figure 4** illustrates the recommended top layer metallization and via placements used for a substrate utilizing high-frequency SMA connectors. **Figure 5** details the four-layer PCB stack-up using a 2.5 mil (.0635 mm) Astra MT77 RF core.

Important parameters for the CPWG transmission lines are as follows:

- RFC transitions from a 50Ω input to a 60Ω line of length 200 µm
- RF1 through RF4 ports transition from 50Ω transmission lines to 68Ω lines of length 450 µm

The same TRL parameters of PRT-80235 are configured for this EVK board at the chip transitions and fan out with 50Ω TRLs to the RF connectors.

Improved RF performance of PCBs configured with connectors can be achieved by following the best practice of utilizing micro vias within a specified diameter from the connector RF pins. (The recommended EVK layout can be downloaded from the pSemi website.)

Figure 4 ▪ PRT-80002 PCB Substrate Metallization and Via Pattern Used for High-frequency SMA Connectors

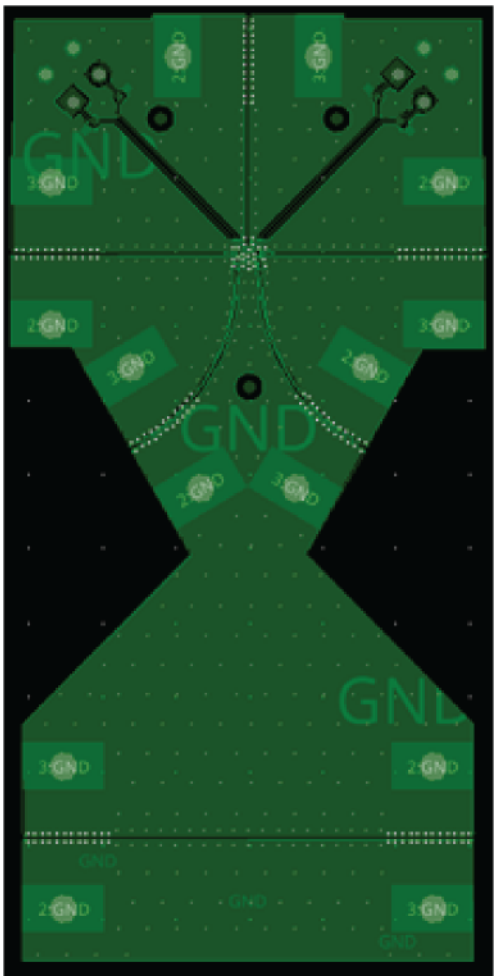
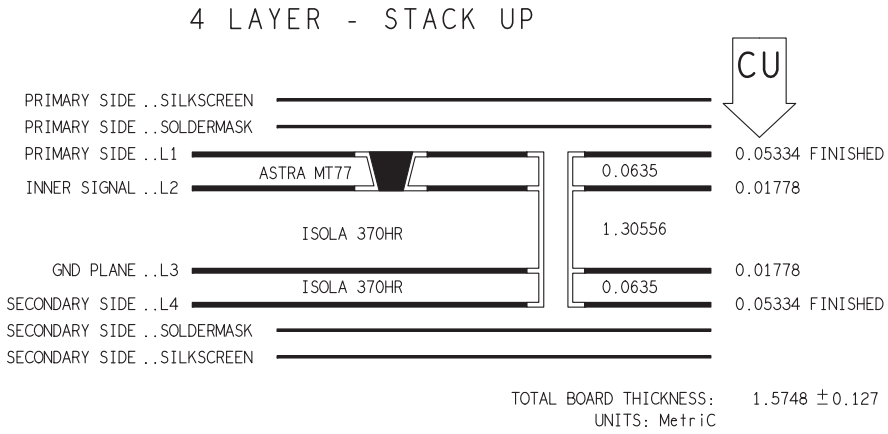


Figure 5 ▪ PRT-80002 Printed Circuit Board Composition



There is an important distinction between a PCB configured with a high-frequency connector and RF probe-able boards. Measured results of PCBs with connectors exhibit high-frequency RF performance limitations related to the limitations of the RF connector to board transitions.

Improved RF performance of PCBs configured with connectors an be achieved by using a core-only PCB instead of a core plus laminate buildup.

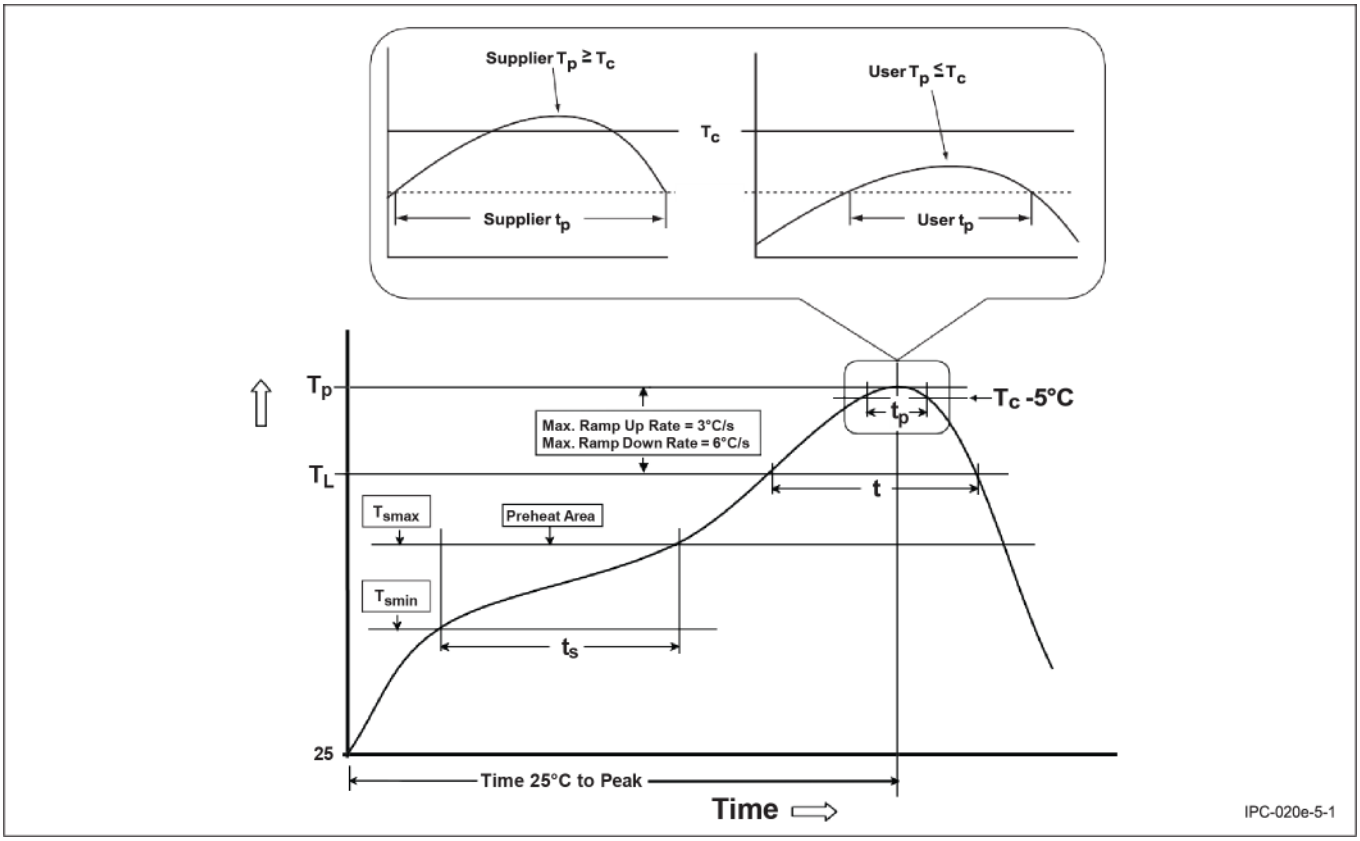
Assembly Process

Assembling the PE42545 leverages common SMD solder reflow techniques. **Figure 6** shows a reflow profile suitable for use with an PCB substrate and which follows a recognized JEDEC profile. Observe the following recommendations when attaching the PE42545.

- No solder paste needs to be printed.
- Apply a thin layer of flux by stencil printing.
- Pick and place the die and align it on the substrate.
- Conduct reflow using a controlled reflow profile. (Refer to JSTD020E-01.)
- Lead-based reflow: Table 4-1
- Lead-free reflow: Table 4-2
- Reflow definition: Section 5.6 and Figure 5-1
- Check for alignment and voids in joint using x-ray inspection after reflow.

Observe these assembly guidelines when attaching the PE42545 PCB substrate: Be aware to the substrate material, its glassivation temperature, and the material coefficient of thermal expansion (CTE) when defining a reliable reflow profile. Excessive soak times or temperatures may cause significant assembly yield issues.

Figure 6 ▪ Generalized Reflow Profile (Reference JEDECJ-STD-020E)



Recommendations for Attaching the PE42545 on a PCB

When defining a reliable reflow profile, pay attention to the PCB substrate material, its glassivation temperature and the various CTEs. Excessive soak times or temperatures can cause significant assembly yield issues and potentially laminate delamination.

Table 3 through **Table 5** list assembly-related process parameters that can help define an assembly flow for specific high-frequency PCB substrates. When refining a suitable reflow profile and assembly process, also consider other components on the same PCB, the PCB substrate temperature limitations, and the PCB board design and its thermal properties.

Table 3 ▪ PE42545 Assembly-related Parameters

Parameter	PE42545	Unit	Comments
Max reflow temperature, TP	≥260	°C	JEDEC J-STD-020D.1 Table 4-2
Max dwell at TP	10	sec	JEDEC J-STD-020D.1 Table 5-2
Recommended flux			
Pb-free solder ball	Tin-95.5/Ag-3.5/Cu-1 (%)		SAC 351 solder definition
Min landing size	90	µm	
Solder stop max thickness	25	µm	
Solder stop diameter	120	µm	
Solder paste particle size	Not recommended		If deemed necessary, type 5, 15–25 µm particle size
Stencil thickness	60	µm	
Stencil aperture diameter	180	µm	
CTE (worst case X, Y, Z)	6-7	ppm/°C	
Underfill	Not recommended		If deemed necessary, a low-loss, low-dielectric constant underfill is recommended.

Table 4 ▪ Assembly Related Parameters for Common High-frequency PCB Substrates

Parameter		Astra MT77	Rogers 4350	Rogers 4003	Unit
Max reflow temperature, TP		288	≥260	≥260	°C
Max dwell at TP		10	10	10	sec
Glassivation temperature, TG		200	>280	>280	°C
CTE (worst case X, Y, Z)	X	12	10	11	ppm/°C
	Y	12	12	14	
	Z	60	32	46	

Table 5 ▪ Reflow Profile Parameter Recommendations

Parameter	Pb-free Assembly	Unit	Comments
Preheat temperature	150-200	°C	
Preheat time	60-120	sec	
Ramp up rate	3	°C/sec	
Liquidous temperature, TL	217	°C	SAC 351 melting point
Time above TL	60-150	sec	
Peak temperature, TP	260	°C	
Time within 5 °C of TP	10-30	sec	
Time 25 °C to TP	6-8	min	
Ramp down rate	3-6	°C/sec	
Note: * Source is JEDEC J-STD-020E.			

Measured Performance

Figure 7 shows the RF1/RF4 insertion loss behavior to 67 GHz of the PE42545 when mounted to the PCB probe substrate carrier and measured in an RF probe configuration. **Figure 8** shows the isolation out to 67 GHz and the RFC and RF1/RF4 active port return losses.

Figure 7 ▪ Insertion Loss PE42545 on PCB Probe Substrate

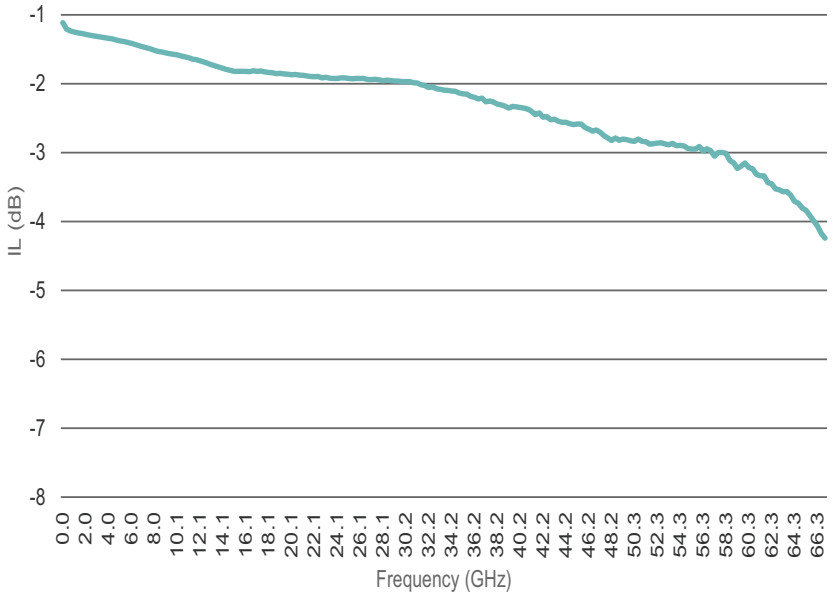


Figure 8 ▪ Isolation and Return Loss of PE42545 on PCB Probe Substrate

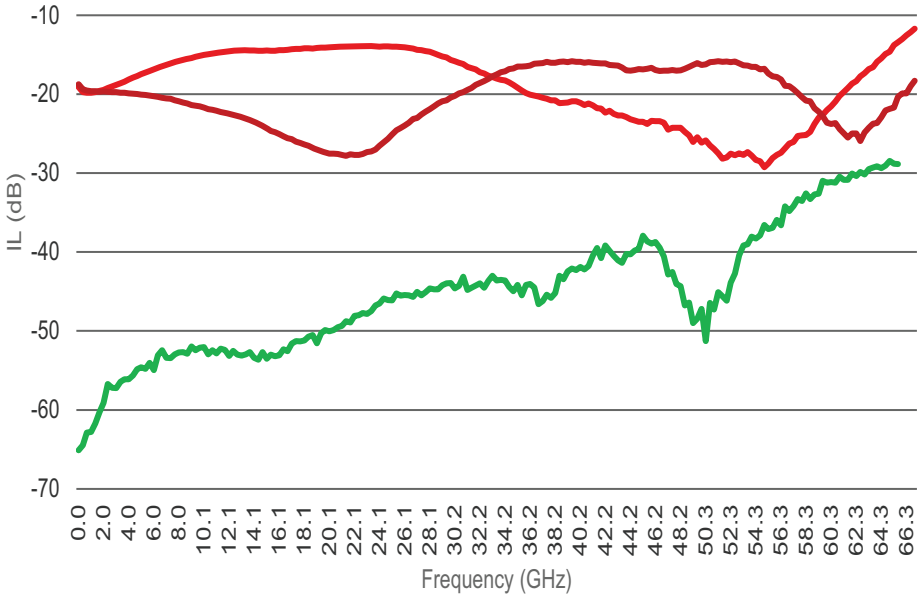


Figure 9 and **Figure 10** show probe vs. connector EVK measurements. Connector EVKs show slightly less Insertion loss past 45 GHz and can be attributed to RF probe transitions made for the PCB substrate as well as additional 50Ω line lengths to the probe points. The connector EVK data fully de-embeds the 50Ω line lengths. Similarly, the return loss correlates probe vs. connector EVKs with the exception of VSWR affects, due to the longer TRL feeds of the connector EVK as well the connector to PCB board transitions.

Figure 9 ▪ Insertion Loss of PE42545 on PCB Probe Substrate vs. PCB EVK Substrate with RF Connectors

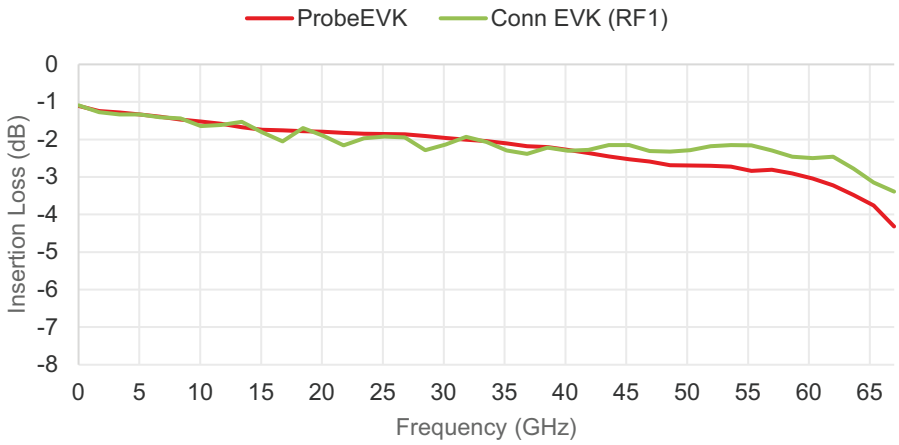
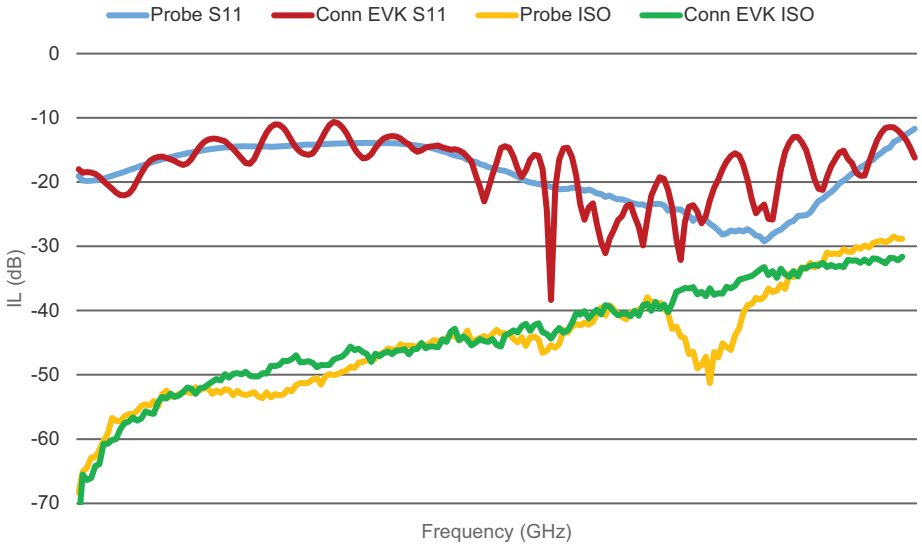


Figure 10 ▪ Isolation and Return Loss of PE42545 on PCB Probe Substrate vs. PCB EVK Substrate with RF Connectors



Conclusion

PE42545 is the newest millimeter wave switch from pSemi. The switch delivers competitive insertion loss, exceptional isolation, and high linearity and power handling, along with the uniformity and availability that UltraCMOS affords. To achieve high performance at these frequencies, however, extreme care must be taken to eliminate stray parasitics affecting the RF channel.

The guidelines and best practices in this application note enable users to obtain optimum performance from the PE42545. It includes descriptions of landing patterns in different substrate technologies, which show comparable performance up to 67 GHz. Complete CAD files of the physical layouts are available from pSemi's website to help integrate the PE42545 into higher-level assemblies and systems.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark