PE42562

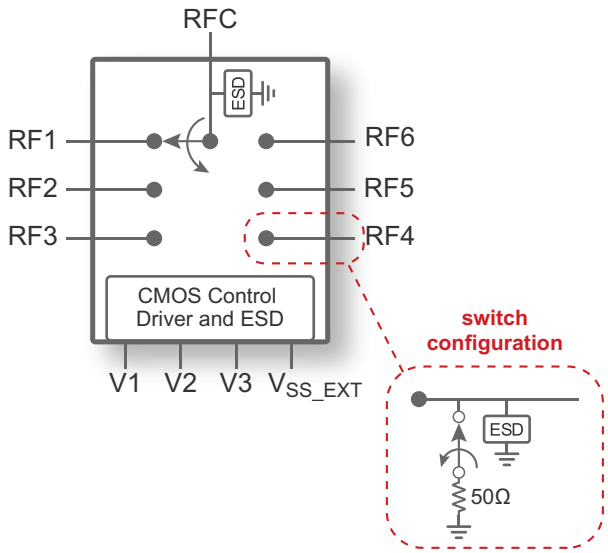
Document Category: Product Specification

UltraCMOS® SP6T RF Switch, 9 kHz–8 GHz

Features

- High isolation: 35 dB @ 6 GHz
- Low insertion loss: 1.1 dB @ 6 GHz
- Fast switching time of 210 ns
- Power handling of 33 dBm CW
- Logic select (LS) pin provides maximum control logic flexibility
- Terminated all-off state mode
- External V_{SS} pin to eliminate spur
- Packaging – 24-lead 4 × 4 × 0.85 mm QFN

Figure 1 ▪ PE42562 Functional Diagram



Applications

- Test and measurement
- Wireless applications up to 8 GHz
- Filter bank switching
- RF signal routing

Product Description

The PE42562 is a HaRP™ technology-enhanced absorptive SP6T RF switch that supports a frequency range from 9 kHz to 8 GHz. An external V_{SS} pin is available for bypassing the internal negative voltage generator in order for the PE42562 to deliver spur-free performance. It delivers high isolation, low insertion loss and fast switching time, making this device ideal for filter bank switching and RF signal routing in test and measurement (T&M) and wireless applications up to 8 GHz. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42562 is manufactured on pSemi's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS}

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for PE42562

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage (V1, V2, V3, LS)	–0.3	3.6	V
RF input power (RFC–RFX, 50Ω)		See **Figure 2**	dBm
RF input power into terminated ports, CW(1) (RFX, 50Ω)		See **Figure 2**	dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		1000	V
ESD voltage CDM, all pins(3)		1000	V

Notes:
1) 100% duty cycle, all bands, 50Ω.
2) Human body model (MIL-STD 883 Method 3015).
3) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE42562. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Conditions for PE42562

Parameter	Min	Typ	Max	Unit
Normal mode (V_{SS_EXT} = 0V)(1)				
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}		120	200	µA
Bypass mode (V_{SS_EXT} = –3.0V)(2)				
Supply voltage, V_{DD} (Table 3 spec. compliance applies for $V_{DD} \geq 3.4V$)	3.1	3.4	5.5	V
Supply current, I_{DD}		80	160	µA
Negative supply voltage, V_{SS_EXT}	–3.3	–3.0	–2.7	V
Negative supply current, I_{SS}	–40	–16		µA
Normal or Bypass mode				
Digital input high (V1, V2, V3, LS)	1.17		3.6	V
Digital input low (V1, V2, V3, LS)	–0.3		0.6	V
Digital input current V1, V2, V3 LS			 5 10	 µA µA
RF input power, CW (RFC–RFX)(3)			See Figure 2	dBm
RF input power, pulsed (RFC–RFX)(4)			See Figure 2	dBm
RF input power into terminated ports, CW (RFX)(3)			See Figure 2	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 7) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 7) to bypass and disable internal negative voltage generator.
3) 100% duty cycle, all bands, 50Ω.
4) Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Electrical Specifications

Table 3 provides the PE42562 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified. Normal mode[1] is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode[2] is at V_{DD} = 3.4V and V_{SS_EXT} = –3.0V.

Table 3 ▪ PE42562 Electrical Specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			9 kHz		8 GHz	As shown
Insertion loss[3]	RFC–RF1/6	9 kHz–100 MHz		0.7	0.9	dB
		100 MHz–1 GHz		0.8	1.0	dB
		1–2 GHz		0.9	1.2	dB
		2–4 GHz		0.9	1.5	dB
		4–6 GHz		1.1	1.9	dB
		6–8 GHz		1.6	2.8	dB
	RFC–RF2/5	9 kHz–100 MHz		0.8	1.0	dB
		100 MHz–1 GHz		0.9	1.1	dB
		1–2 GHz		0.9	1.3	dB
		2–4 GHz		1.0	1.6	dB
		4–6 GHz		1.3	2.3	dB
		6–8 GHz		1.3	2.4	dB
	RFC–RF3/4	9 kHz–100 MHz		0.8	1.0	dB
		100 MHz–1 GHz		0.9	1.1	dB
		1–2 GHz		1.0	1.3	dB
		2–4 GHz		1.1	1.7	dB
		4–6 GHz		1.2	2.2	dB
		6–8 GHz		1.3	2.2	dB
Isolation[3]	RFC–RF1/6	9 kHz–100 MHz	61	65		dB
		100 MHz–1 GHz	45	47		dB
		1–2 GHz	40	42		dB
		2–4 GHz	34	36		dB
		4–6 GHz	29	32		dB
		6–8 GHz	27	30		dB
	RFC–RF2/5	9 kHz–100 MHz	64	68		dB
		100 MHz–1 GHz	52	55		dB
		1–2 GHz	47	51		dB
		2–4 GHz	42	44		dB
		4–6 GHz	30	34		dB
		6–8 GHz	29	34		dB
	RFC–RF3/4	9 kHz–100 MHz	64	68		dB
		100 MHz–1 GHz	51	53		dB
		1–2 GHz	46	48		dB
		2–4 GHz	38	40		dB
		4–6 GHz	33	35		dB
		6–8 GHz	29	31		dB

Table 3 ▪ PE42562 Electrical Specifications (Cont.)

Parameter	Path	Condition	Min	Typ	Max	Unit
Return loss (active port)	RFC–RF1/6	9 kHz–100 MHz		25		dB
		100 MHz–1 GHz		24		dB
		1–2 GHz		24		dB
		2–4 GHz		21		dB
		4–6 GHz		26		dB
		6–8 GHz		13		dB
	RFC–RF2/5	9 kHz–100 MHz		24		dB
		100 MHz–1 GHz		23		dB
		1–2 GHz		20		dB
		2–4 GHz		18		dB
		4–6 GHz		15		dB
		6–8 GHz		16		dB
	RFC–RF3/4	9 kHz–100 MHz		24		dB
		100 MHz–1 GHz		23		dB
		1–2 GHz		18		dB
		2–4 GHz		15		dB
		4–6 GHz		12		dB
		6–8 GHz		12		dB
Return loss (RFC port)	RFC–RF1/6	9 kHz–100 MHz		25		dB
		100 MHz–1 GHz		23		dB
		1–2 GHz		24		dB
		2–4 GHz		23		dB
		4–6 GHz		24		dB
		6–8 GHz		12		dB
	RFC–RF2/5	9 kHz–100 MHz		24		dB
		100 MHz–1 GHz		23		dB
		1–2 GHz		21		dB
		2–4 GHz		19		dB
		4–6 GHz		20		dB
		6–8 GHz		18		dB
	RFC–RF3/4	9 kHz–100 MHz		24		dB
		100 MHz–1 GHz		23		dB
		1–2 GHz		19		dB
		2–4 GHz		16		dB
		4–6 GHz		13		dB
		6–8 GHz		13		dB

Table 3 ▪ PE42562 Electrical Specifications (Cont.)

Parameter	Path	Condition	Min	Typ	Max	Unit
Return loss (terminated port)	RF1/6	9 kHz–100 MHz		16		dB
		100 MHz–1 GHz		15		dB
		1–2 GHz		15		dB
		2–4 GHz		15		dB
		4–6 GHz		18		dB
		6–8 GHz		21		dB
	RF2/5	9 kHz–100 MHz		16		dB
		100 MHz–1 GHz		15		dB
		1–2 GHz		15		dB
		2–4 GHz		15		dB
		4–6 GHz		18		dB
		6–8 GHz		19		dB
	RF3/4	9 kHz–100 MHz		16		dB
		100 MHz–1 GHz		15		dB
		1–2 GHz		15		dB
		2–4 GHz		15		dB
		4–6 GHz		16		dB
		6–8 GHz		19		dB
Relative insertion phase[4]	RF2–RF1 (RF5–RF6)	1 GHz	–2.6	–1.3	0	Deg
		2 GHz	–4.7	–2.4	–0.1	Deg
		4 GHz	–7.5	–3.4	0.~~7~~8	Deg
		6 GHz	–9.4	–2.8	3.8	Deg
		8 GHz	–1.4	4.4	10.~~0~~1	Deg
	RF3–RF1 (RF4–RF6)	1 GHz	–3.0	–2.1	–1.~~2~~3	Deg
		2 GHz	–5.8	–4.0	–2.1	Deg
		4 GHz	–9.3	–5.6	–1.9	Deg
		6 GHz	–11.2	–5.7	–0.~~2~~3	Deg
		8 GHz	–10.2	–1.0	8.2	Deg
Input 1dB compression point[5]	RFC–RFX			See **Figure 2**		dBm
Input 0.1dB compression point[5]	RFC–RFX			See **Figure 2**		dBm
Input IP2	RFC–RFX	5 MHz		75		dBm
		100 MHz–8 GHz		105		dBm
Input IP3	RFC–RFX	5 MHz		53		dBm
		100 MHz–8 GHz		60		dBm
RF T_{RISE}/T_{FALL}		10%/90% RF		100	130	ns
Settling time		50% CTRL to 0.05 dB final value		560	920	ns
Switching time		50% CTRL to 90% or 10% of RF		210	270	ns

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 7) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 7) to bypass and disable internal negative voltage generator.
3) Insertion loss and isolation performance can be improved by a good RF ground on the LS pin (pin 1).
4) Defined with S-parameters, relative insertion phase (RFX–RF1) = $\angle S_{(x+1)1} - \angle S_{21}$, where incident Port-1 is RFC, response Port-2 = RF1, and response Port-(x+1) = RFx.
5) The input 1dB and 0.1dB compression points are linearity figures of merit. Refer to **Table 2** for the RF input power (50Ω).

Switching Frequency

The PE42562 has a maximum 25 kHz switching frequency in normal mode (pin 7 tied to ground). A faster switching frequency is available in bypass mode (pin 7 tied to V_{SS_EXT}). The rate at which the PE42562 can be switched is then limited to the switching time as specified in **Table 3**.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spur-free Performance

The PE42562 spur fundamental occurs around 5 MHz. Its typical performance in normal mode is –162 dBm/Hz (pin 7 tied to ground), with 30 kHz bandwidth. If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 7).

Hot-Switching Capability

The maximum hot switching capability of the PE42562 is 20 dBm above 100 MHz. Hot switching occurs when RF power is applied while switching between RF ports.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 ▪ Thermal Data for PE42562

Parameter	Typ	Unit
Ψ_{JT}	23	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	63	°C/W

Control Logic

Table 5 provides the control logic truth table for PE42562.

Table 5 ▪ Truth Table for PE42562

LS[1]	V3	V2	V1	RFC–RF1	RFC–RF2	RFC–RF3	RFC–RF4	RFC–RF5	RFC–RF6
0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF
0	1	0	0	OFF	ON	OFF	OFF	OFF	OFF
0	0	1	0	OFF	OFF	ON	OFF	OFF	OFF
0	1	1	0	OFF	OFF	OFF	ON	OFF	OFF
0	0	0	1	OFF	OFF	OFF	OFF	ON	OFF
0	1	0	1	OFF	OFF	OFF	OFF	OFF	ON
1	1	0	1	ON	OFF	OFF	OFF	OFF	OFF
1	0	0	1	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	0	OFF	OFF	ON	OFF	OFF	OFF
1	0	1	0	OFF	OFF	OFF	ON	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	ON	OFF
1	0	0	0	OFF	OFF	OFF	OFF	OFF	ON
X[2]	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF

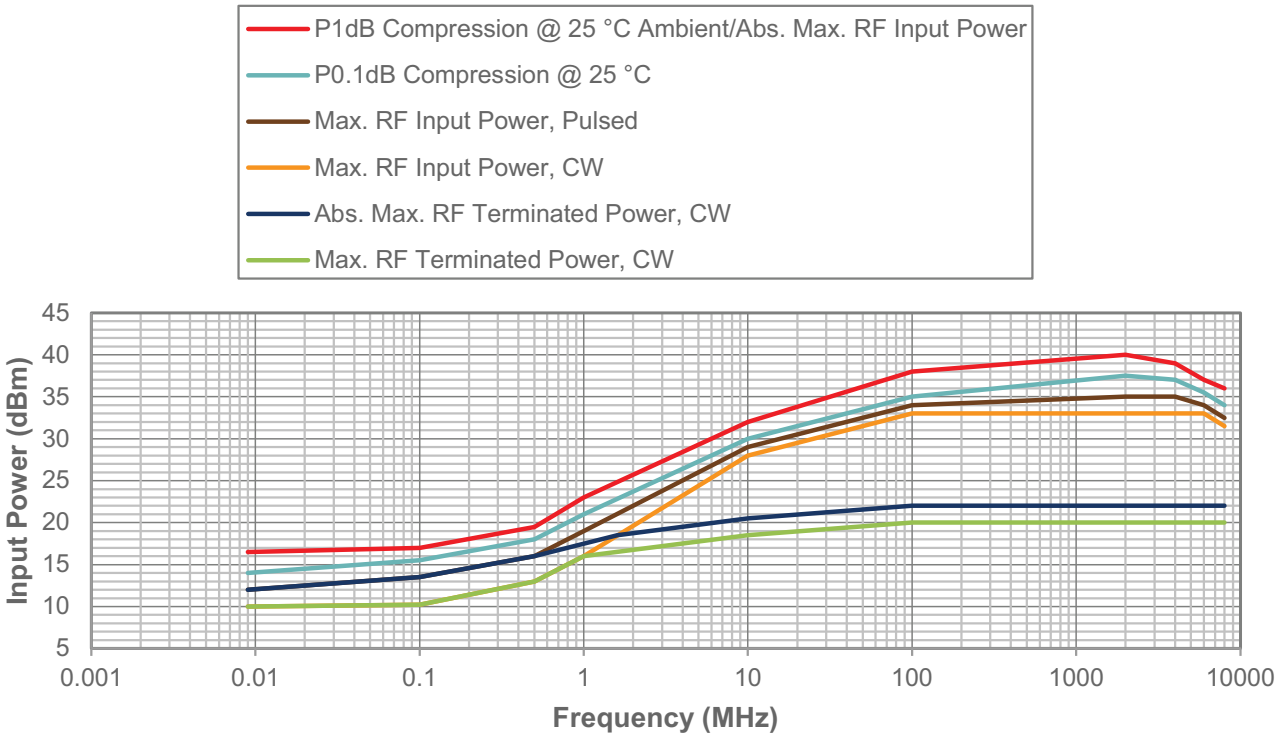
Notes:

1) LS has an internal 1 MΩ pull-up resistor to logic high. Connect LS to GND externally to generate a logic 0. Leaving LS floating will generate a logic 1.
2) LS = don't care, V3 = 0, V2 = V1 = 1, all ports are terminated to provide an all isolated state.

Power De-rating Curve

Figure 2 shows the power de-rating curve showing P1dB compression, P0.1dB compression, maximum RF input power (pulsed), maximum RF input power (CW), absolute maximum RF terminated power (CW), and maximum RF terminated power (CW).

Figure 2 ▪ Power De-rating Curve, 9 kHz–8 GHz, –40 °C to +105 °C Ambient, 50?



Isolation Matrix

Table 6 provides RFC-to-port isolation and Table 7 provides port-to-port isolation at +25 °C, V_{DD} = 3.3V (Z_S = Z_L = 50Ω). Normal mode(1) is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode(2) is at V_{DD} = 3.4V and V_{SS_EXT} = –3.0V.

Table 6 ▪ RFC-to-Port Isolation

"ON" Port	Frequency	Isolation (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	9 kHz–100 MHz	–	69	68	88	87	79
	100 MHz–1 GHz	–	62	53	66	64	57
	1–2 GHz	–	57	48	60	58	51
	2–4 GHz	–	48	40	54	52	45
	4–6 GHz	–	37	35	50	46	42
	6–8 GHz	–	34	31	47	45	38
RF2	9 kHz–100 MHz	67	–	69	88	86	77
	100 MHz–1 GHz	52	–	60	66	64	56
	1–2 GHz	46	–	57	60	57	50
	2–4 GHz	39	–	49	53	52	45
	4–6 GHz	32	–	43	50	46	42
	6–8 GHz	30	–	37	47	46	40
RF3	9 kHz–100 MHz	65	68	–	88	85	77
	100 MHz–1 GHz	47	55	–	66	63	55
	1–2 GHz	42	51	–	60	57	50
	2–4 GHz	36	44	–	53	52	45
	4–6 GHz	33	40	–	49	47	42
	6–8 GHz	31	36	–	46	47	40
RF4	9 kHz–100 MHz	73	84	88	–	68	66
	100 MHz–1 GHz	51	62	65	–	56	50
	1–2 GHz	45	56	59	–	51	45
	2–4 GHz	40	49	53	–	46	39
	4–6 GHz	37	46	49	–	38	35
	6–8 GHz	34	44	45	–	37	33
RF5	9 kHz–100 MHz	73	84	89	69	–	68
	100 MHz–1 GHz	51	62	65	60	–	57
	1–2 GHz	45	56	59	57	–	52
	2–4 GHz	40	49	53	50	–	44
	4–6 GHz	37	45	49	41	–	33
	6–8 GHz	34	43	46	38	–	33
RF6	9 kHz–100 MHz	74	84	87	68	69	–
	100 MHz–1 GHz	52	62	66	54	65	–
	1–2 GHz	46	57	60	48	60	–
	2–4 GHz	40	49	53	41	51	–
	4–6 GHz	37	46	49	35	34	–
	6–8 GHz	33	42	46	31	35	–

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 7) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 7) to bypass and disable internal negative voltage generator.

Table 7 ▪ Port-to-Port Isolation

"ON" Port	Frequency	Isolation (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	9 kHz–100 MHz	–	65	67	89	89	88
	100 MHz–1 GHz	–	47	51	69	71	64
	1–2 GHz	–	41	45	63	65	60
	2–4 GHz	–	35	39	57	60	53
	4–6 GHz	–	31	34	52	47	45
	6–8 GHz	–	29	30	49	47	43
RF2	9 kHz–100 MHz	65	–	64	91	92	89
	100 MHz–1 GHz	46	–	45	70	75	74
	1–2 GHz	41	–	39	64	69	72
	2–4 GHz	35	–	34	58	64	63
	4–6 GHz	32	–	30	53	50	51
	6–8 GHz	29	–	27	50	50	51
RF3	9 kHz–100 MHz	67	65	–	90	92	91
	100 MHz–1 GHz	51	47	–	70	78	80
	1–2 GHz	46	41	–	64	72	79
	2–4 GHz	40	36	–	58	66	68
	4–6 GHz	37	33	–	53	51	54
	6–8 GHz	33	30	–	50	51	54
RF4	9 kHz–100 MHz	90	92	89	–	65	67
	100 MHz–1 GHz	77	82	70	–	47	51
	1–2 GHz	65	75	65	–	42	45
	2–4 GHz	56	66	58	–	36	39
	4–6 GHz	49	52	53	–	32	35
	6–8 GHz	46	53	50	–	31	32
RF5	9 kHz–100 MHz	92	92	89	64	–	64
	100 MHz–1 GHz	85	77	70	45	–	45
	1–2 GHz	70	72	64	39	–	40
	2–4 GHz	57	64	58	34	–	35
	4–6 GHz	48	52	53	30	–	29
	6–8 GHz	46	51	50	27	–	30
RF6	9 kHz–100 MHz	87	91	88	67	65	–
	100 MHz–1 GHz	69	73	69	51	47	–
	1–2 GHz	67	67	63	45	41	–
	2–4 GHz	56	61	57	39	35	–
	4–6 GHz	46	49	52	34	29	–
	6–8 GHz	42	49	49	30	29	–

Typical Performance Data

Figure 3–Figure 20 show the typical performance data at +25 °C, V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 3 ▪ Insertion Loss vs. Frequency (RFC–RFX)

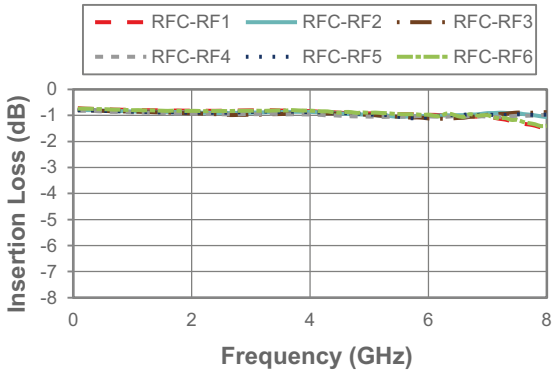


Figure 4 ▪ Insertion Loss vs. Frequency Over Temperature (RFC–RF1)

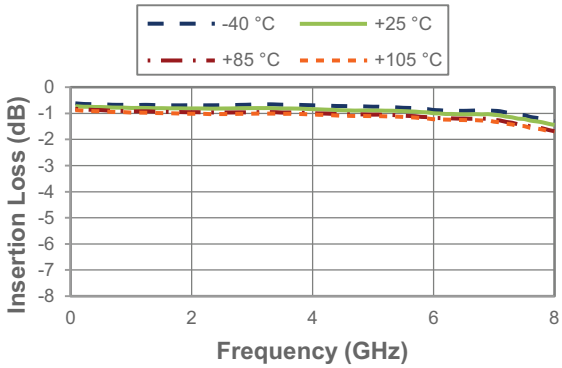


Figure 5 ▪ Insertion Loss vs. Frequency Over V_{DD} (RFC–RF1)

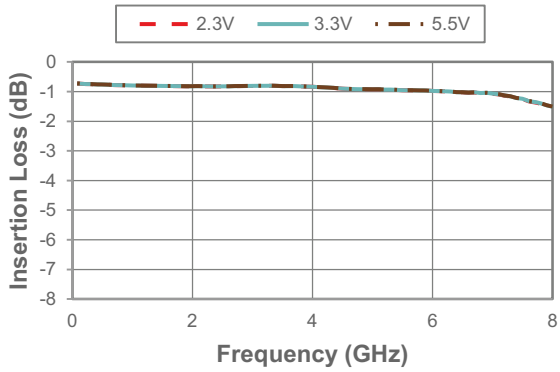


Figure 6 ▪ RFC Port Return Loss vs. Frequency

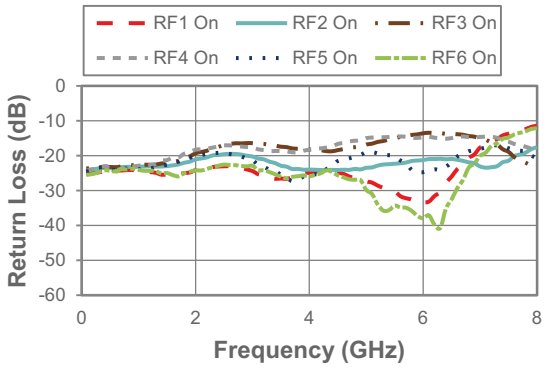


Figure 7 ▪ RFC Port Return Loss vs. Frequency Over Temperature (RF1 On)

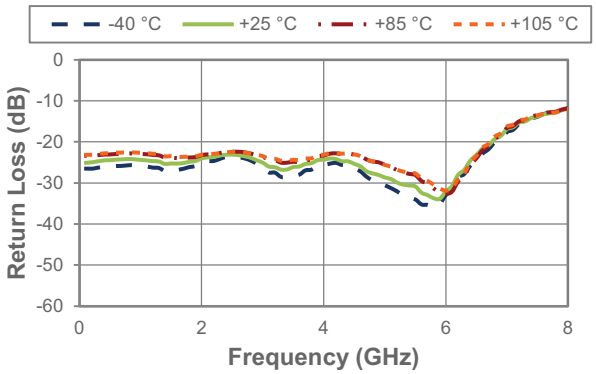


Figure 8 ▪ RFC Port Return Loss vs. Frequency Over V_{DD} (RF1 On)

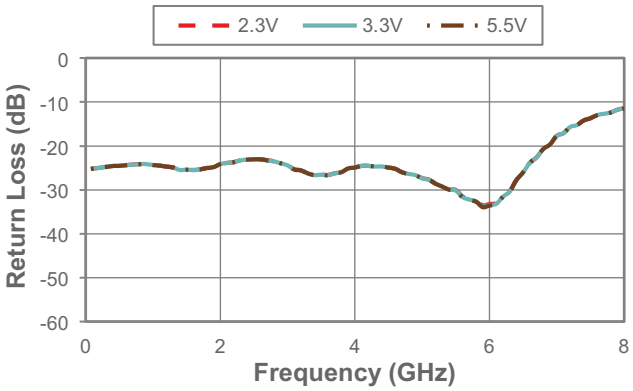


Figure 9 ▪ Active Port Return Loss vs. Frequency

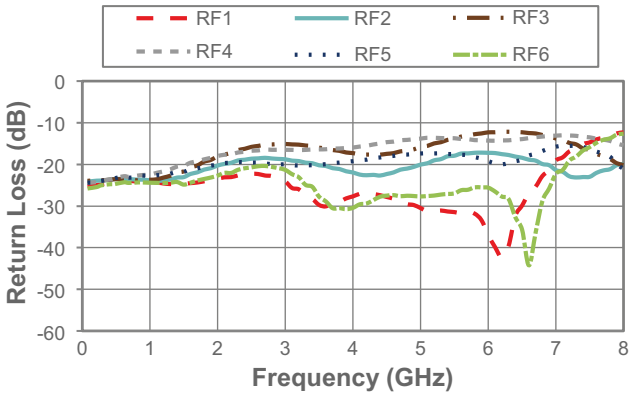


Figure 10 ▪ RF1 Active Port Return Loss vs. Frequency Over Temperature

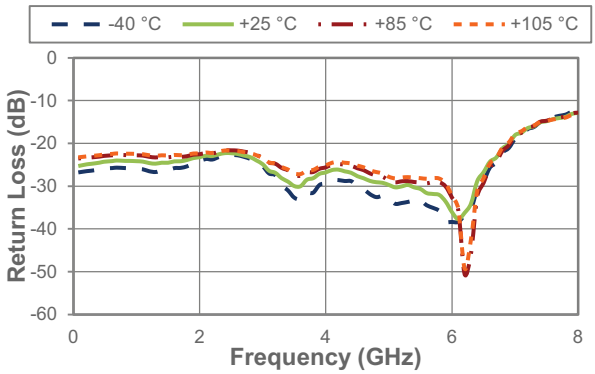


Figure 11 ▪ RF1 Active Port Return Loss vs. Frequency Over V_{DD}

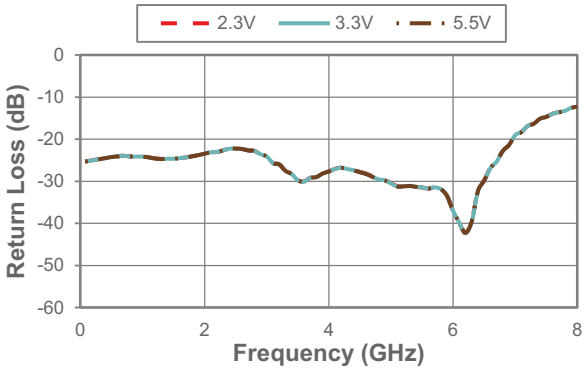


Figure 12 ▪ Terminated Port Return Loss vs. Frequency (RF1 On)

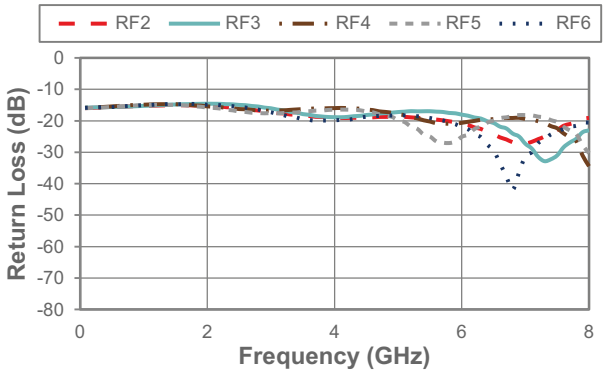


Figure 13 ▪ RF2 Terminated Port Return Loss vs. Frequency Over Temperature (RF1 On)

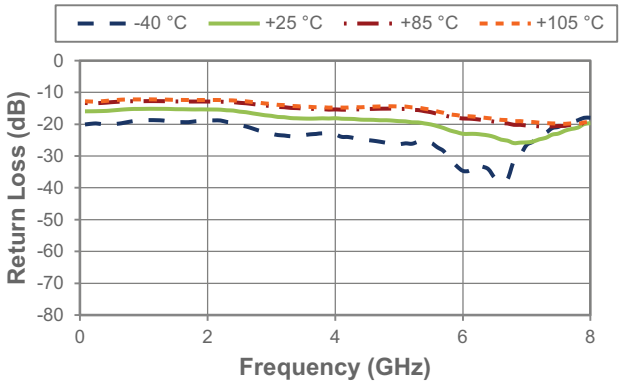


Figure 14 ▪ RF2 Terminated Port Return Loss vs. Frequency Over V_{DD} (RF1 On)

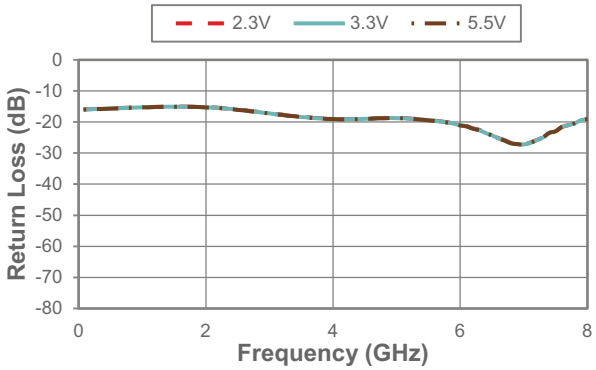


Figure 15 ▪ Isolation vs. Frequency Over Temperature (~~RFX–RFX~~RF1–RF2, RF1 On)

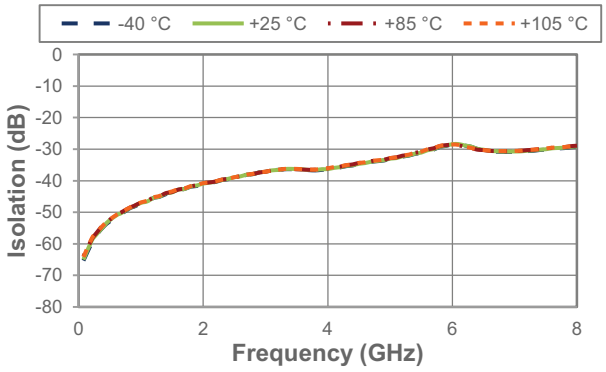


Figure 16 ▪ Isolation vs. Frequency Over V_{DD} (~~RFX–RFX~~RF1–RF2, RF1 On)

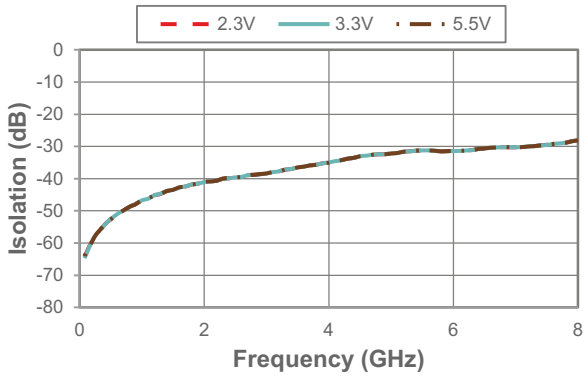


Figure 17 ▪ Isolation vs. Frequency Over Temperature (RFC–RF2, RF1 On)

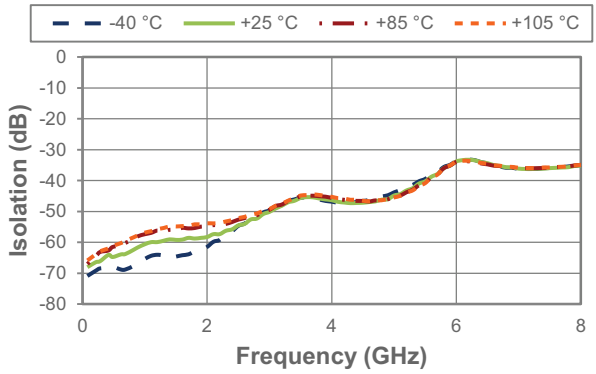


Figure 18 ▪ Isolation vs. Frequency Over V_{DD} (RFC–RF2, RF1 On)

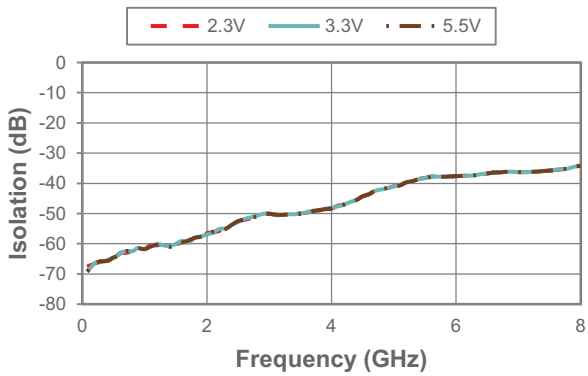


Figure 19 ▪ IIP2 vs. RF Port Measured

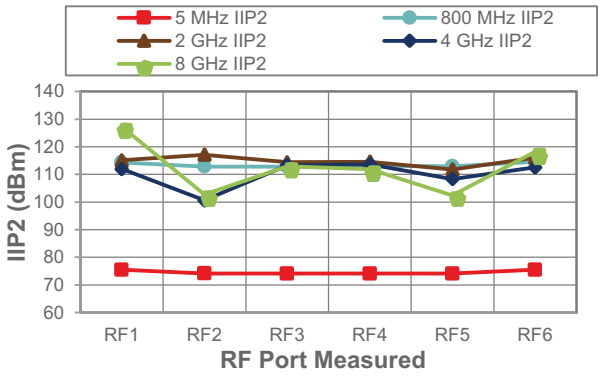
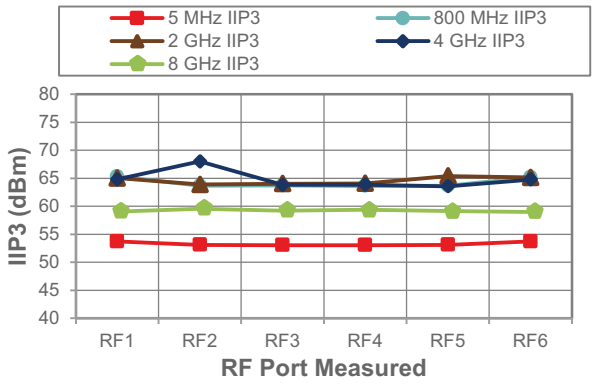


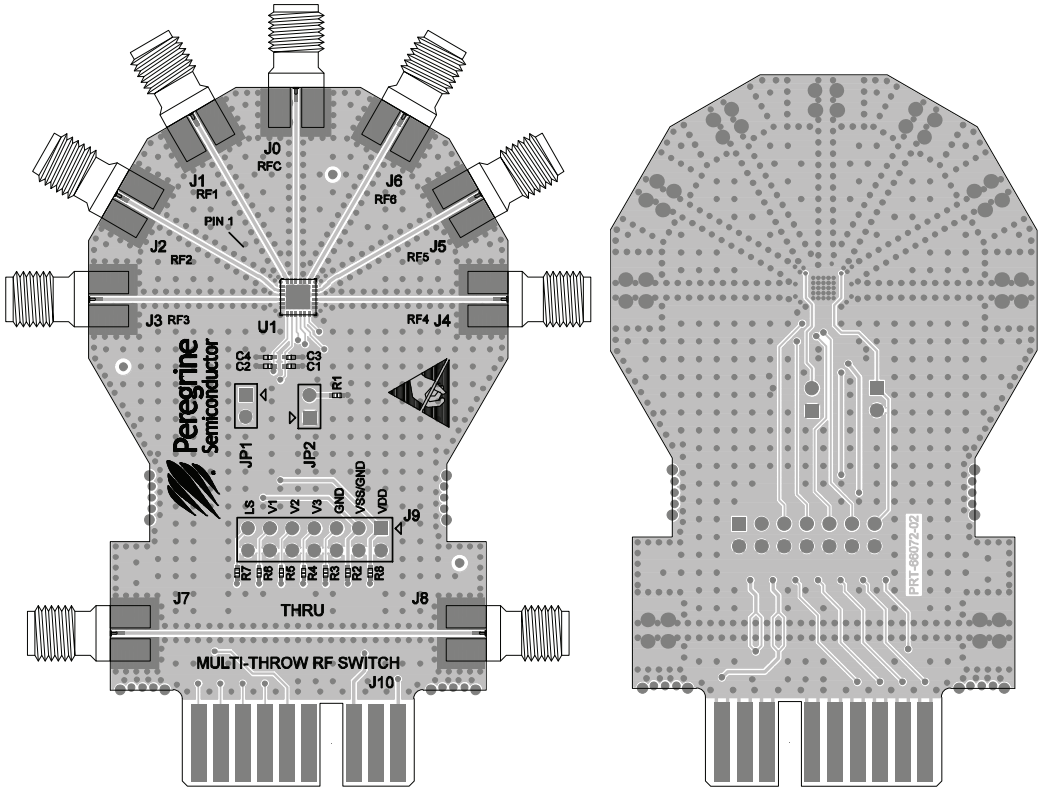
Figure 20 ▪ IIP3 vs. RF Port Measured



Evaluation Kit

The high-throw count RF switch evaluation kit (EVK) includes hardware required to control and evaluate the functionality of the high-throw count switches. The high-throw count RF switch evaluation software can be downloaded at www.psemi.com and requires a PC running Windows® operating system to control the USB interface board. Refer to the *Multi-throw Count RF Switch Evaluation Kit (EVK) User's Manual* for more information.

Figure 21 ▪ Evaluation Board Layout for PE42562



Pin Information

This section provides pinout information for the PE42562. **Figure 22** shows the pin map of this device for the available package. **Table 8** provides a description for each pin.

Figure 22 ▪ Pin Configuration (Top View)

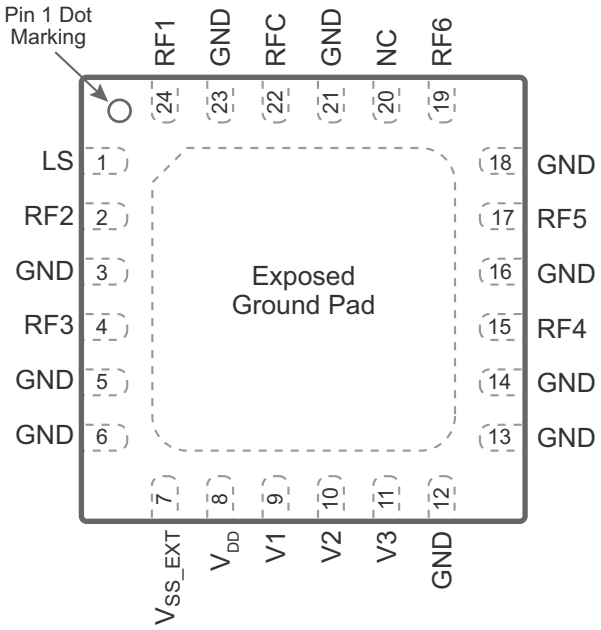


Table 8 ▪ Pin Descriptions for PE42562

Pin No.	Pin Name	Description
1	LS	Logic Select—used to determine the definition for V1, V2 and V3 pins
2	RF2(1)	RF port 2
3, 5, 6, 12–14, 16, 18, 21, 23	GND	Ground
4	RF3(1)	RF port 3
7	V_{SS_EXT}(2)	External V_{SS} negative voltage control
8	V_{DD}	Supply voltage (nominal 3.3V)
9	V1	Digital control logic input 1
10	V2	Digital control logic input 2
11	V3	Digital control logic input 3
15	RF4(1)	RF port 4
17	RF5(1)	RF port 5
19	RF6(1)	RF port 6
20	NC(3)	No connect
22	RFC(1)	RF common port
24	RF1(1)	RF port 1
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) RF pins 2, 4, 15, 17, 19, 22 and 24 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) Use V_{SS_EXT} (pin 7) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 7) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
3) Pin 20 (NC) can be connected to GND or left not connected externally.

Packaging Information

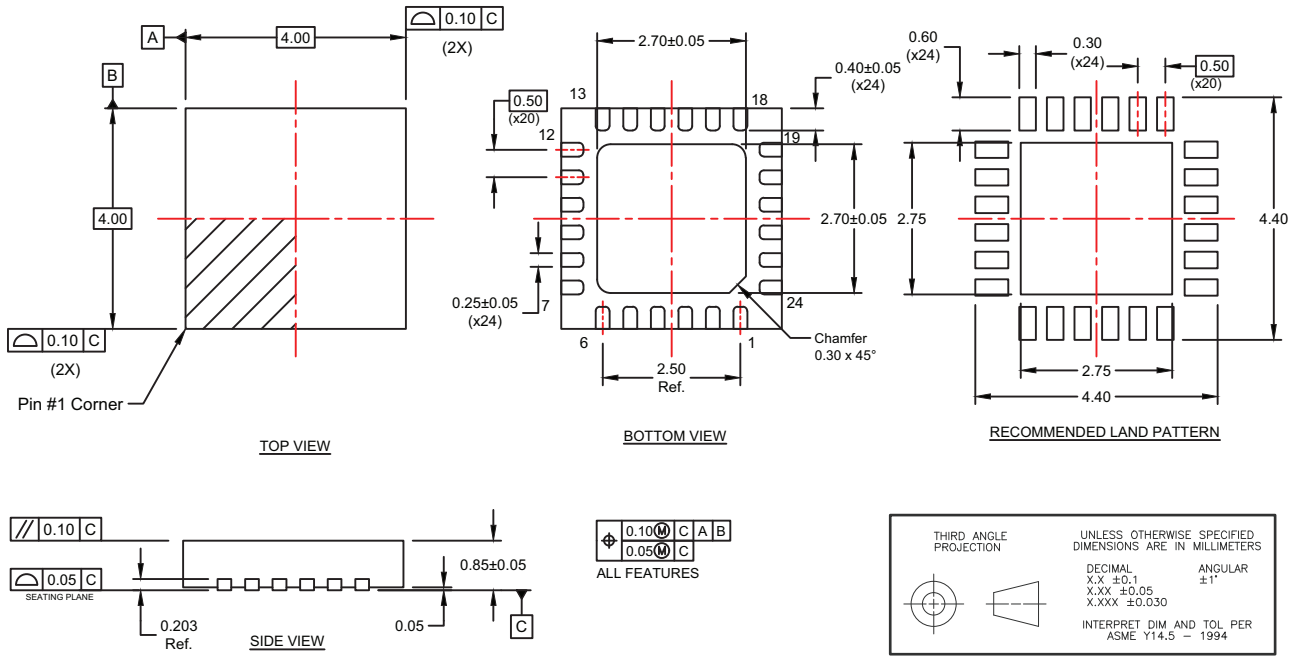
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE42562 in the 24-lead 4 × 4 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 23 ▪ Package Mechanical Drawing for 24-lead 4 × 4 × 0.85 mm QFN



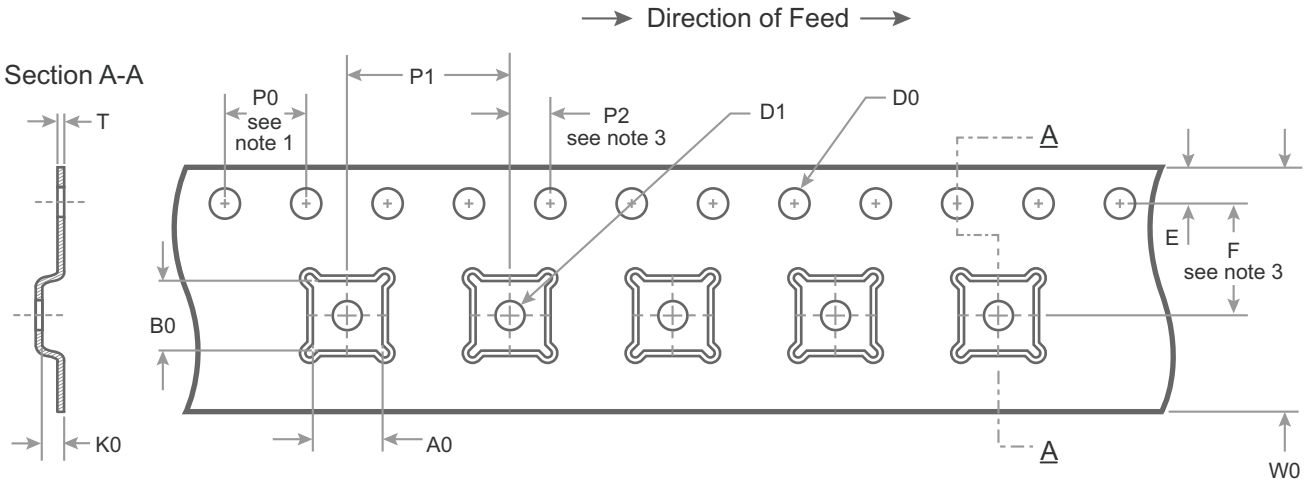
Top-Marking Specification

Figure 24 ▪ Package Marking Specifications for PE42562

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (Maximum six characters)

Tape and Reel Specification

Figure 25 ▪ Tape and Reel Specifications for 24-lead 4 × 4 × 0.85 mm QFN

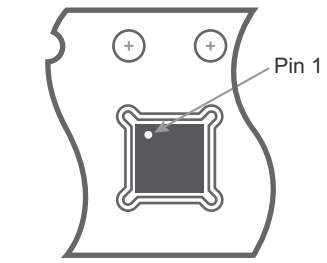


A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

Ordering Information

Table 9 lists the available ordering codes for the PE42562 as well as available shipping methods.

Table 9 ▪ Order Codes for PE42562

Order Codes	Description	Packaging	Shipping Method
PE42562A-X	PE42562 SP6T RF switch	Green 24-lead 4 × 4 mm QFN	500 units/T&R
EK42562-02	PE42562 Evaluation kit	Evaluation kit	1/Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

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