Summary

Peregrine Semiconductor Application Note AN33 demonstrates socket and software compatibility of the 5 bit and 6 bit digital step attenuators products. This family offers high performance attenuation accuracy and linearity using only a single 3 volt supply.

1. Introduction

Typical digital step attenuators (DSA) in GaAs technology require either a single or bipolar 5 Volt supply, and either a +5 or -5 Volt control interface. Peregrine DSA’s require only one +3 volt supply to deliver extremely high linearity and high accuracy. Other features include default power-up attenuation state, user selectable serial, parallel, and direct mode programming, 3 volt CMOS interface, 50 and 75 ohm variations, and very low power consumption. This document describes forward / backward compatibility of the 5 bit and 6 bit models.

Features

- 5 & 6 bit models
- Common flexible parallel and serial programming interfaces
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and Linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 50Ω impedance
- Packaged in a 20 Lead 4x4mm QFN

Figure 1. Typical 6 bit evaluation schematic

Figure 2. 20 pin / 4x4 QFN
A 6 bit attenuator can be installed in a 5 bit design. The highlighted pins are different for 5 bit users as explained below.

### 6-bit Attenuator

<table>
<thead>
<tr>
<th>Pin</th>
<th>C16</th>
<th>C8</th>
<th>C4</th>
<th>C2</th>
<th>C1</th>
<th>C0.5</th>
<th>Attenuation State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reference Loss</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.5 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8 dB</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>16 dB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>31.5 dB</td>
</tr>
</tbody>
</table>

Note: Not all possible combinations of C0.5-C8 are shown.

### 5-bit Attenuator

<table>
<thead>
<tr>
<th>Pin</th>
<th>C16</th>
<th>C8</th>
<th>C4</th>
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<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Reference Loss</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.5 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8 dB</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>16 dB</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>31.5 dB</td>
</tr>
</tbody>
</table>

Note: Not all possible combinations of C0.5-C8 are shown.

### 5-bit 31 dB Serial Timing

Figure 3. 6-bit 31.5 dB Serial Timing

Figure 4. 5-bit 15.5 dB Serial Timing

Figure 5. 5-bit 31 dB Serial Timing
2. Generic Hardware Design Consideration

The 5 bit and 6 bit parts share a common pinout. The only differences between the 5 and 6 bit parts are the two specific pins associated with the Direct Mode 0.5 dB and 16 dB steps.

**Direct Mode**
In Direct Mode the pin assigned to an unavailable step becomes a Don’t Care.

- 5 Bit, 0.5 dB LSB Pin 1, C16 on the 6 bit device, becomes inactive or Don’t Care.
- 5 Bit, 1 dB LSB Pin 20, C0.5 on the 6 bit device, becomes inactive or Don’t Care.

***For the 6-bit part to emulate the 5-bit part, the “Don’t Care” pin should be held Lo.***
***For designs that may upgrade from 5-bit to 6-bit, the “Don’t Care” pins can be routed to zero ohm resistor initially hooked to ground, with provision to connect to controller.***

**Serial Mode**
The 5 and 6 bit parts use a common 6 bit serial word format. The first bit, the MSB, corresponds to the 16 dB step and the LSB corresponds to the 0.5 dB step.

- 5 Bit, 0.5 dB LSB Device operates on either a 5 or 6 bit word. Optional 6th MSB is ignored and the state is set by the last 5 bits sent. If the designer anticipates a possible upgrade to a 6 bit, 31.5 dB part, then a 6 bit word preserves full software compatibility.
- 5 Bit, 1 dB LSB Device requires 6 bit word. The 0.5 dB bit is received but ignored.

1. The 5-bit 31 dB part in **serial** mode uses a similar clock/data string. Use Figure 4, noting 6 clocks are required, and five data bits position as shown.
2. The 5-bit 31 dB part in **parallel** mode uses the table in Figure 4. Note data bit pin C0.5 is unused.
3. The 5-bit 15.5 dB part in **serial** mode uses a similar clock/data string. Use Figure 5, noting 6 clocks are required, and five data bits position as shown.
4. The 5-bit 15.5 dB part in **parallel** mode uses the table in Figure 5. Note data bit pin C16 is unused.

*** NOTE: Controlling the 6th bit position in a 5-bit attenuator will put the part into an unknown state.
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