Using the PE29102 Driver as a Differential Voltage Translator

Application Note 70

Summary

This application notes describes how to configure the PE29102 UltraCMOS® High-speed FET Driver as an adjustable level, high slew rate, differential voltage translator and shows an example of this implementation.

Introduction

The Peregrine Semiconductor PE29102 is a high-speed driver that can be configured to provide a high slew rate differential signal with adjustable output levels. In this configuration, the PE29102 can be used to provide the control signal requirement for the Peregrine PE42525 60 GHz RF switch. The PE29102 provides the required ±3.0V control signal, with a high slew rate that matches the high switching speed of the PE42525 switch.

Figure 1 and **Figure 2** show the functional diagram for each device. The PE29102 differential outputs are the HSG and LSG signals used to drive the PE42525 V1 and V2 control signals. **Table 1** shows the PE42525 control truth table.

Figure 1 • *PE29102 Functional Diagram*

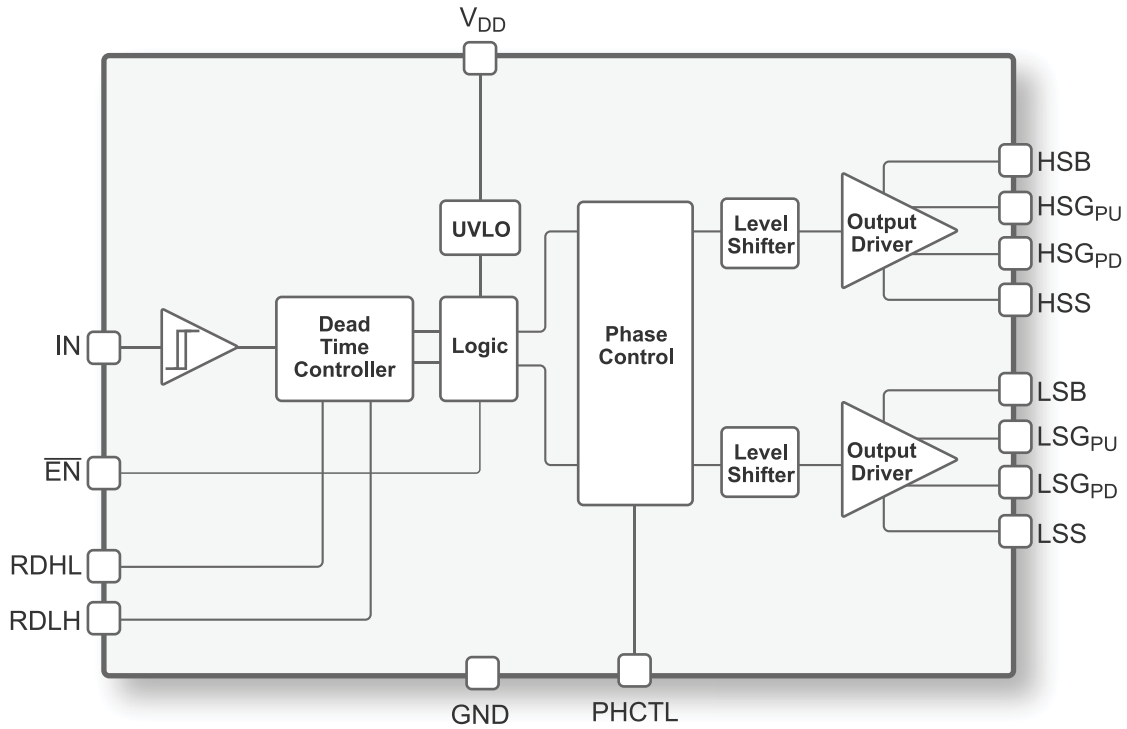


Figure 2 • *PE42525 Functional Diagram*

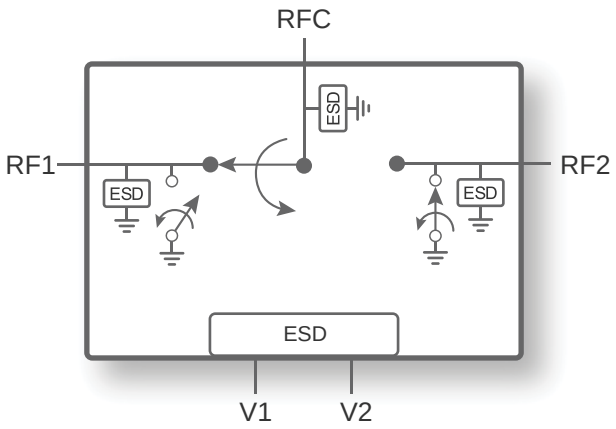
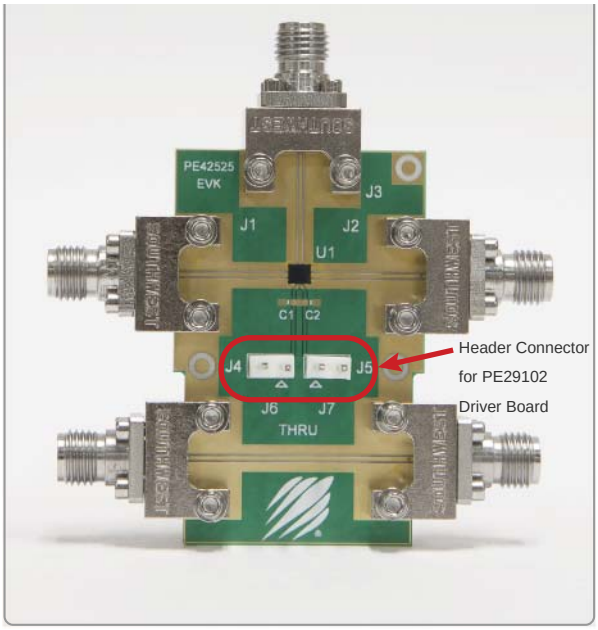


Table 1 • *Truth Table for PE42525*

V1	V2	RF1	RF2	
–3.0V	–3.0V	OFF	OFF	
–3.0V	+3.0V	OFF	ON	Normal operation
+3.0V	–3.0V	ON	OFF	
+3.0V	+3.0V	ON	ON	

Figure 3 shows the PE42525 evaluation printed circuit board (PCB) EK42525-88 40 GHz. The RF ports are the SMA connectors, with the logic drive provided by the white header connectors indicated.

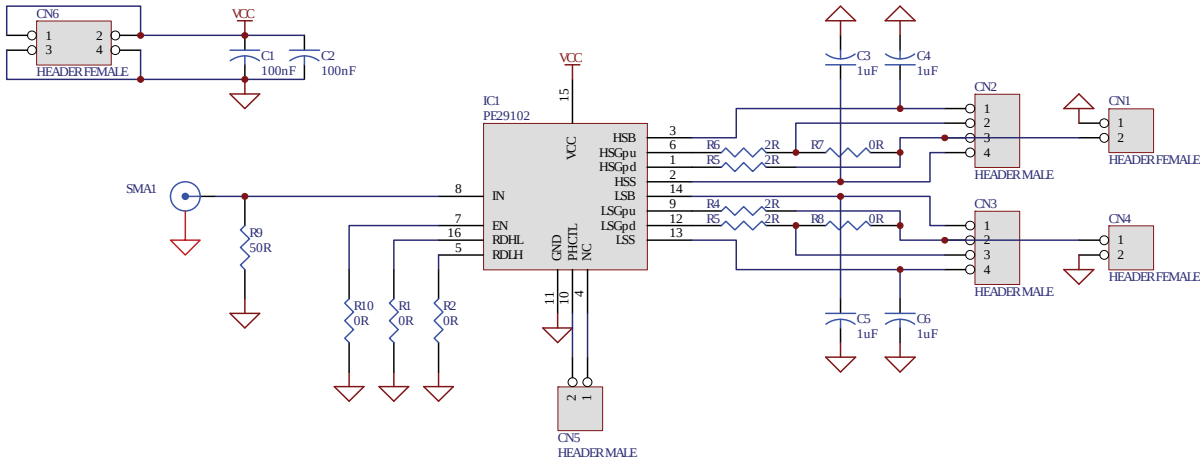
Figure 3 • *EK42525-88 40 GHz PCB*



Driver PCB

The modified PE29102 configuration is shown in **Figure 4**.

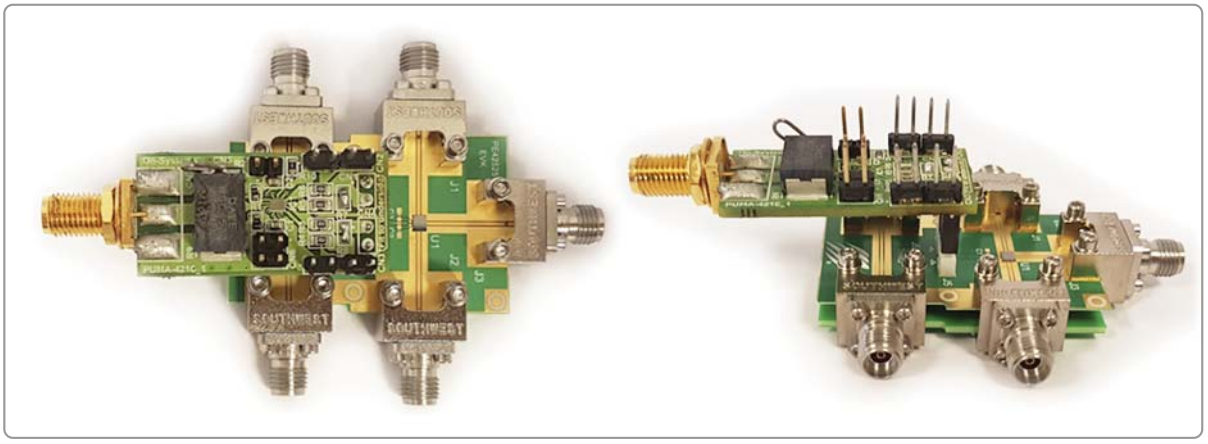
Figure 4 • *Rider PCB Schematic*



This circuit is used to create a daughter “Rider” board that fits onto the PE42525 EVK, as shown in **Figure 5**. Using a single-ended CMOS pulse input, the PE29102 converts the single-ended logic input into differential drive signals defined by the PE29102 HSB/LSB and HSS/LSS inputs. In this case, +3.0V and -3.0V are used to define the output signal levels and the resultant inputs to the PE42525 V1 and V2 control pins.

Note: Pin10 PHCTL has a weak pull down and can be left floating or tied to 0V using a jumper on CN5.

Figure 5 • *Modified Rider PE29102 Circuit Mounted on the PE42525 EVK*



The solution requires:

- A 0 – 2.5V logic input (on the sma connector)
- 5V for the PE29102

- +3.0V HSB,LSB and –3.0V HSS,LSS supplies for the output signal

Bench Setup

Figure 6 shows the bench setup block diagram.

Figure 6 • *Bench Setup Block Diagram*

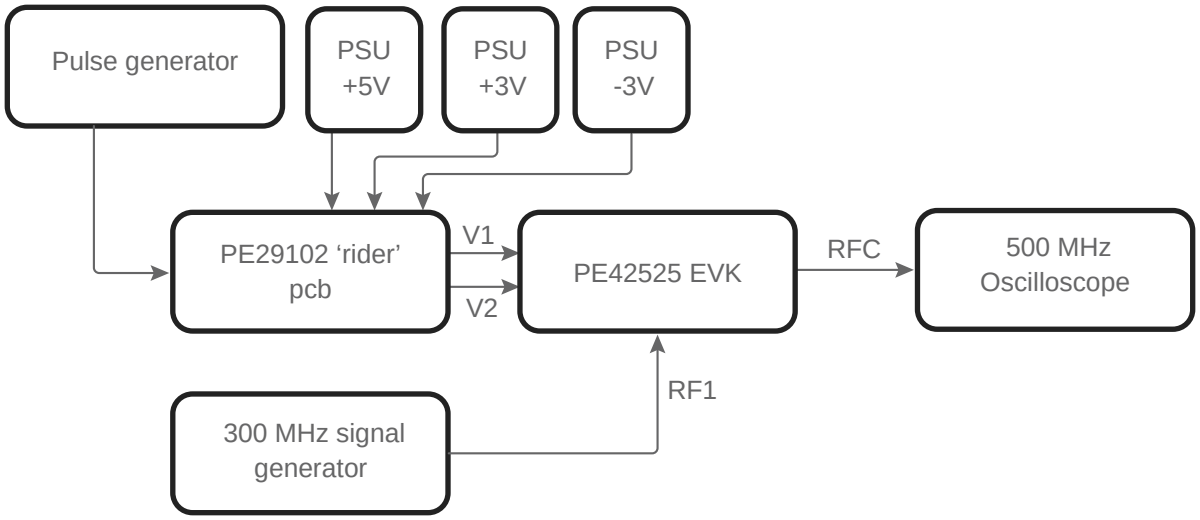


Figure 7 • *Test Setup*

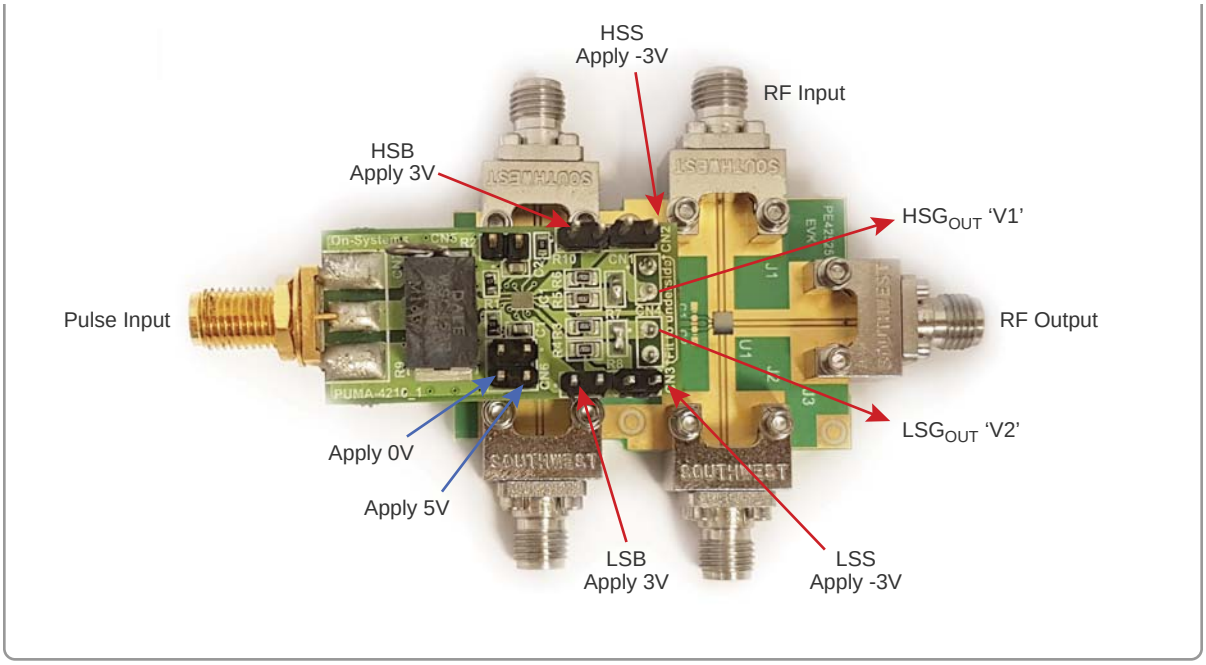


Table 2 lists the board connections required. Table 3 lists the test signal connections.

Table 2 • *Board Connections*

Header Connections	Description
CN6, pins 1 and 2	+5V
CN6, pins 3 and 4	GND
CN2 and CN3, pin 1	+3V
CN2 and CN3, pin 4	–3V
SMA 1	Pulse input

Table 3 • *Oscilloscope Probes in the Bench Setup Block Diagram*

Probe Location	Description
SMA1 input	Pulse input
CN2, pin 3	V1
CN3, pin 2	V2
PE42522 RFC output	RF pulse signal output

Signals

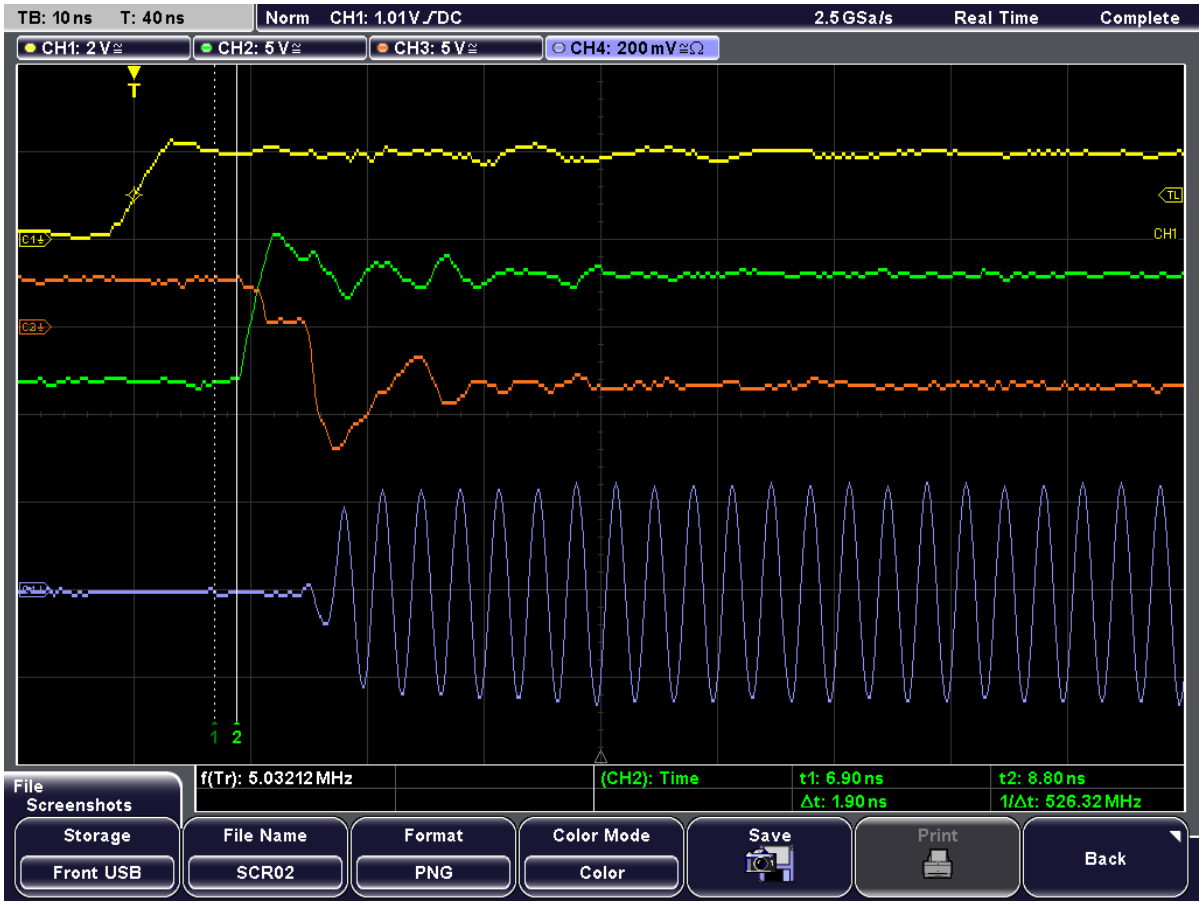
The following signals apply to this application.

- Pulse generator: 100 kHz to 20 MHz (also used for oscilloscope trigger)
- V1, V2 ±3V differential outputs (measured)
- RF1: 300 MHz tone, 0 dBm.
- RFC: switched 300 MHz tone (measured)

Measurement Results

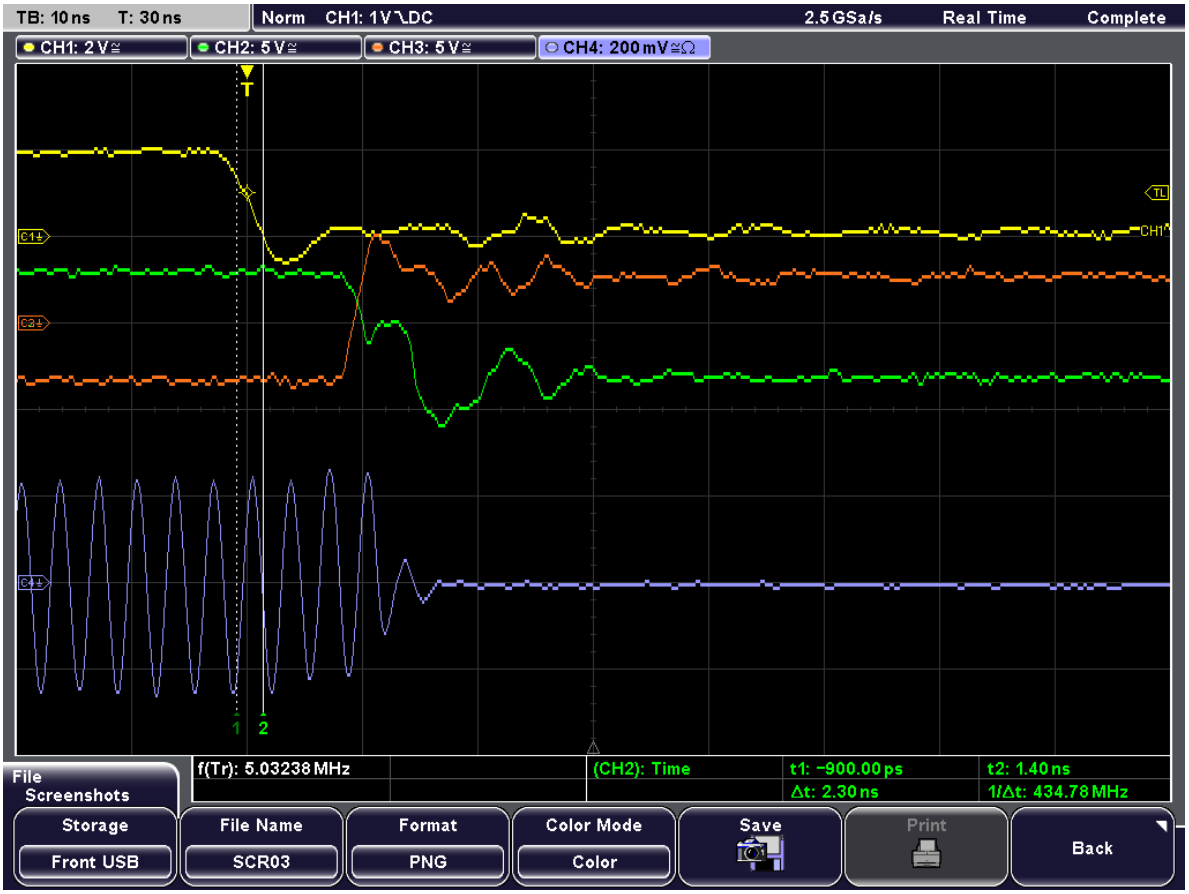
Figure 8 and Figure 9 show the measurement results.

Figure 8 • *ON*(*)



Note: * Legend
Yellow = logic input
Green = V1
Orange = V2
Blue = RF signal at switch output

Figure 9 • *OFF*(*)



Note: * Legend
Yellow = logic input
Green = V1
Orange = V2
Blue = RF signal at switch output

Conclusion

The PE29102 switch is used to drive the PE42525 logic inputs. It provides a high slew rate differential control signal for the PE42525 at the required voltages, and uses the PE29102 rise and fall times to realize the fast switching time of the PE42525 60 GHz RF switch.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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