

Using Peregrine's High-Speed FET Drivers

Application Note 71



Summary

This application note highlights design guidelines and circuit layout techniques when using Peregrine Semiconductor's high-speed field-effect transistor (FET) drivers with enhancement-mode gallium nitride (GaN) transistors. Some basic driver principles and layout considerations are covered as well as specific application examples.

Introduction

The evolution of new technologies, such as wide-bandgap semiconductors (WBGs) is paving the way for smaller, faster, and more efficient power management solutions. GaN transistors are enabling applications, such as wireless power transfer (WPT), class-D audio, and light detection and ranging (LiDAR), that favor solutions offering reduced physical size, weight, and cost.

One of the distinguishing features of GaN transistors is their ability to operate at much higher frequencies than silicon metal-oxide semiconductor field-effect transistors (Si MOSFETs), due to their smaller capacitance and lower on-resistance. Higher switching frequency offers the benefits of smaller magnetics. Increasing the switching frequency requires a driver with lower propagation delay, accurate matching between channels, and minimum parasitic inductance. Consequently, the driver and printed circuit board (PCB) layout require special attention.

Principles of High-Speed Driver Design

Gate Characteristics

Enhancement-mode GaN transistors have lower operating and peak gate voltage ratings than their silicon counterparts. The recommended operating gate-source voltage for the transistor varies based on manufacturer specifications, but is generally in the range of 5–6V. The gate driver must be able to supply a low voltage within the operating limits of the transistor. Exceeding these limits may permanently damage the devices.

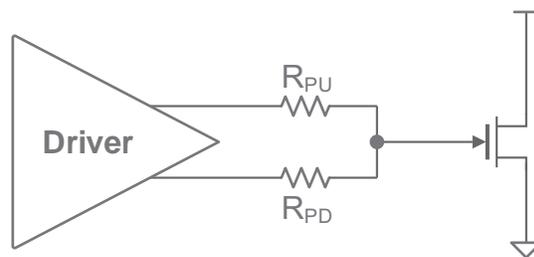
Because GaN transistors are capable of faster switching speeds, the driver should not be the limitation of their performance. High-speed drivers have fast switching edges, resulting in higher slew rates (dv/dt). Additional inductance in the gate drive path can reduce performance by creating voltage overshoot resulting in increased ringing and peaking that can exceed device limitations.

Gate Resistors

Ideally, there would be no inductance in the gate drive path. Realistically, the inductance becomes more prominent in PCB layouts as the switching frequency increases. One method of counteracting the parasitic inductance is to add a damping resistor in series with the gate drive output and the transistor gate to slow down the slew rate. Although the peaking can be controlled by reducing the edge rate, the switching losses will also increase.

A disadvantage to using a single gate resistor is that both rising and falling slew rates are uniformly affected. Due to asymmetry in the waveform edges, it would be desirable to adjust a gate drive pull-up resistance to control the slew rate during turn-on and a gate pull-down resistance to minimize the impedance during turn-off. A driver with separate pull-up and pull-down outputs would allow for a higher gate pull-up resistor and a lower gate pull-down resistor to control both the turn-on and turn-off waveforms independently and to optimize switching loss, electromagnetic interference (EMI), and overshoot without adding unwanted loss (**Figure 1**).

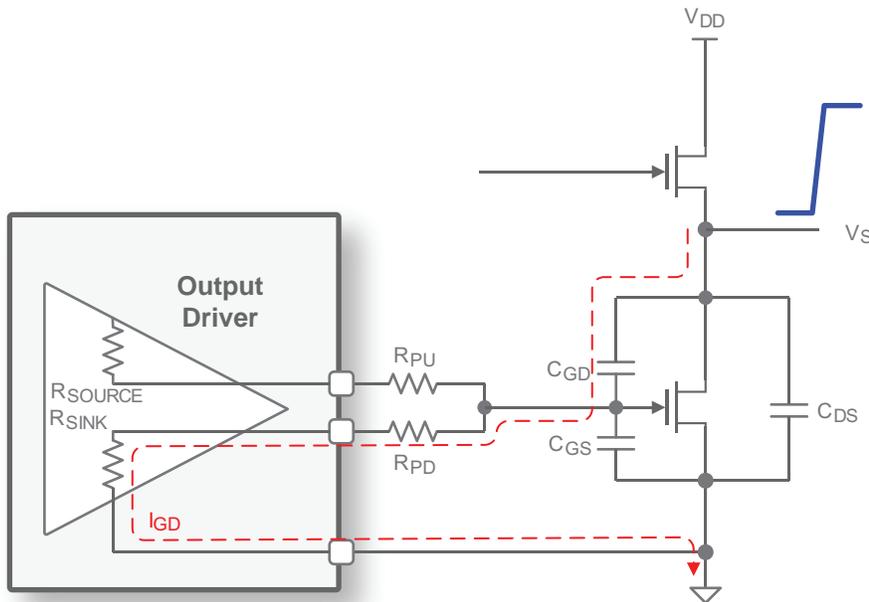
Figure 1 ▪ Driver with Separate Pull-Up and Pull-Down Outputs



Low Impedance Gate Drive

Another event associated with high slew rate is the potential to turn on the transistor prematurely. When the drain-to-source capacitor (C_{DS}) is charging, high current can flow through the gate-to-drain capacitance (C_{GD}) and charge the gate-to-source capacitance (C_{GS}) above V_{th} value. This Miller turn-on effect can result in an undesirable shoot through condition. A low-value pulldown resistor (for example, from 1–2 ohm) on the gate can help keep the gate voltage below the V_{th} value during Miller coupling through C_{GD} . A driver with low R_{SINK} , as shown in **Figure 2**, can reduce sensitivity to Miller turn-on.

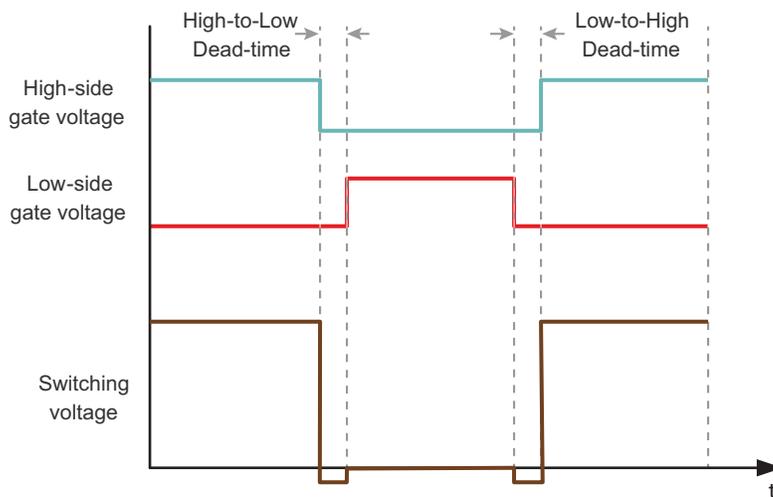
Figure 2 ▪ Low Impedance Drive Circuit



Dead Time Control

Optimizing the dead time between one transistor turning off and the other turning on will improve efficiency (Figure 3). Minimum dead time is recommended for highest efficiency for synchronous driving. Reducing the dead time too much can cause an undesired shoot-through condition. A driver with separate high-side and low-side dead-time controls offers adjustability for both hard and soft switching applications.

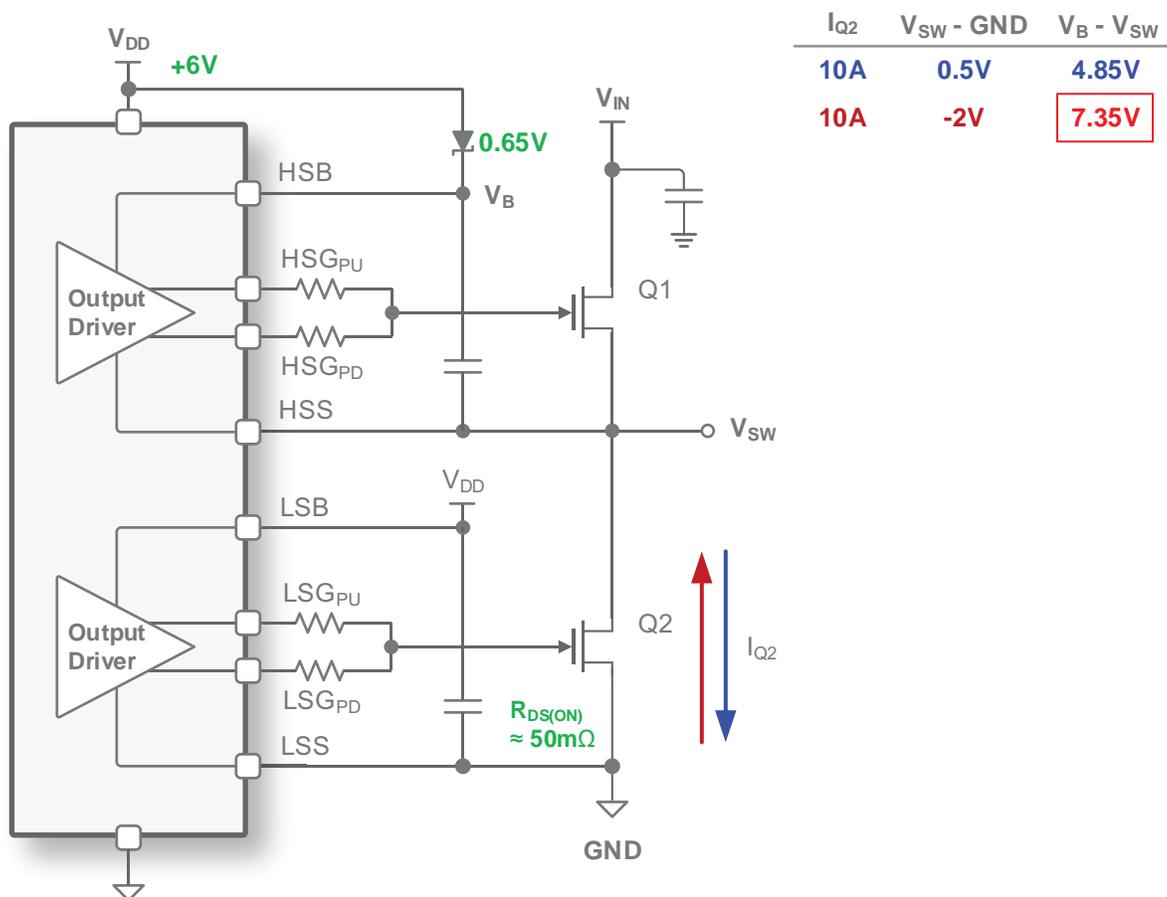
Figure 3 ▪ Half-Bridge Switching Waveforms Showing Dead-Time Region



High-Side Gate Overvoltage

Most half-bridge topologies use a simple bootstrap method with diode and capacitor to generate the gate voltage for the high side drive. This floating or high-side supply works well with most Si MOSFET half-bridge applications but may not be able to provide accurate gate voltage regulation for enhancement mode GaN transistors due to overcharging of the bootstrap capacitor during reverse conduction in dead-time periods (Figure 4).

Figure 4 ■ High-Side Gate Overvoltage with Bootstrap Topology



For applications where the GaN transistor reverse conduction can be significantly longer than the bootstrap diode turn-on time, such as with longer dead times and high load conditions, the switching node voltage (Vsw) can swing from approximately -2V when current flows in reverse conduction to 0.5V for forward conduction. The resulting overvoltage on the high-side supply may exceed the specified operating range of the transistor. In such cases, some form of bootstrap supply regulation is required.¹

1. D. Reusch, M. de Rooij, "Evaluation of Gate Drive Overvoltage Management Methods for Enhancement Mode Gallium Nitride Transistors", APEC, March 2017, pp. 2459 - 2466.

PE29101 and PE29102 High-Speed Drivers

The PE29101 and PE29102 are high-speed FET drivers designed to control the gates of enhancement mode GaN transistors. The driver outputs are capable of providing switching transition speeds in the sub-nanosecond range for switching applications up to 40 MHz. Peregrine's FET drivers offer the following characteristics for optimum high-speed switching performance:

- High- and low-side FET driver outputs
- Low output pull-down (sink) impedance, 1.5Ω or less (typ.)
- 2A/4A peak source/sink current
- Integrated dead time control
- Fast propagation delay, less than 10 ns (typ.)
- Less than 1 ns rise and fall time
- 3 ns minimum pulse width (typ.)
- Low inductance, small flip chip package

The PE29101 operates from 4V to 6.5V and can support a high side floating supply voltage of 80V. An internal synchronous bootstrap management block is included to limit overcharging of the bootstrap capacitor during reverse conduction.

The PE29101 also features a dead-time adjustment that allows the user to control the timing of the low-side (LS) and high-side (HS) gates to eliminate any large shoot-through currents that could dramatically reduce the efficiency of the circuit and potentially damage the GaN transistors. Two external resistors control the timing of outputs in the dead-time controller block. The dead-time resistors only control the low-side gate (LSG) output; the high-side gate (HSG) output will always equal the duty-cycle of the PWM input.

The PE29102 does not include a bootstrap management block, but operates from 4V to 6V and can support a high side floating supply voltage of 60V. It uses a slightly different timing scheme in the dead time circuitry as the dead-time resistors control both rising edges of the LSG and HSG outputs.

The PE29102 also features a phase control pin that inverts the HSG and LSG outputs. This function is convenient for full-bridge topologies when using two PE29102 drivers for applications such as high-fidelity class D audio amplifiers.

Gate Driver Example 1

Figure 5 shows a half-bridge gate driver evaluation board using a PE29101 with two GS61008P 100 V E-mode GaN transistors¹. The schematic is shown in **Figure 6**. U3 buffers a 50Ω PWM signal that feeds the gate driver U4. Both U3 and U4 are supplied by a 6V regulator (U1). The 6V regulator was chosen to optimize, but not exceed, the maximum gate drive voltage of the transistors or the maximum operating voltage of the driver and buffer IC. Resistors R8 and R10 are pull-up resistors for the HSG and LSG, respectively. Resistors R9 and R11 are pull-down resistors for the HSG and LSG. The gate resistors can be adjusted for slew rate control or to minimize overshoot due to gate loop parasitics. R12 and R13 provide a dead-time adjustment to maximize efficiency and eliminate any large shoot-through currents.

The evaluation board was tested as an open loop synchronous buck DC/DC converter at 48:12V with a 12A load switching at 1 MHz. **Figure 7** shows the efficiency measurements of the half-bridge driver with 4.7Ω pull-up resistors compared with 10Ω pull-up resistors. The pull-down resistors were 1Ω in both cases. The evaluation board achieved a peak efficiency of 96%. **Figure 8** shows the corresponding switch node waveforms. Note that the waveform peaking can be reduced by increasing the gate pull-up resistors at the cost of reducing efficiency.

1. GS61008P datasheet, <http://www.gansystems.com/gs61008p.php>

Figure 5 ■ Half-Bridge Driver Evaluation Board

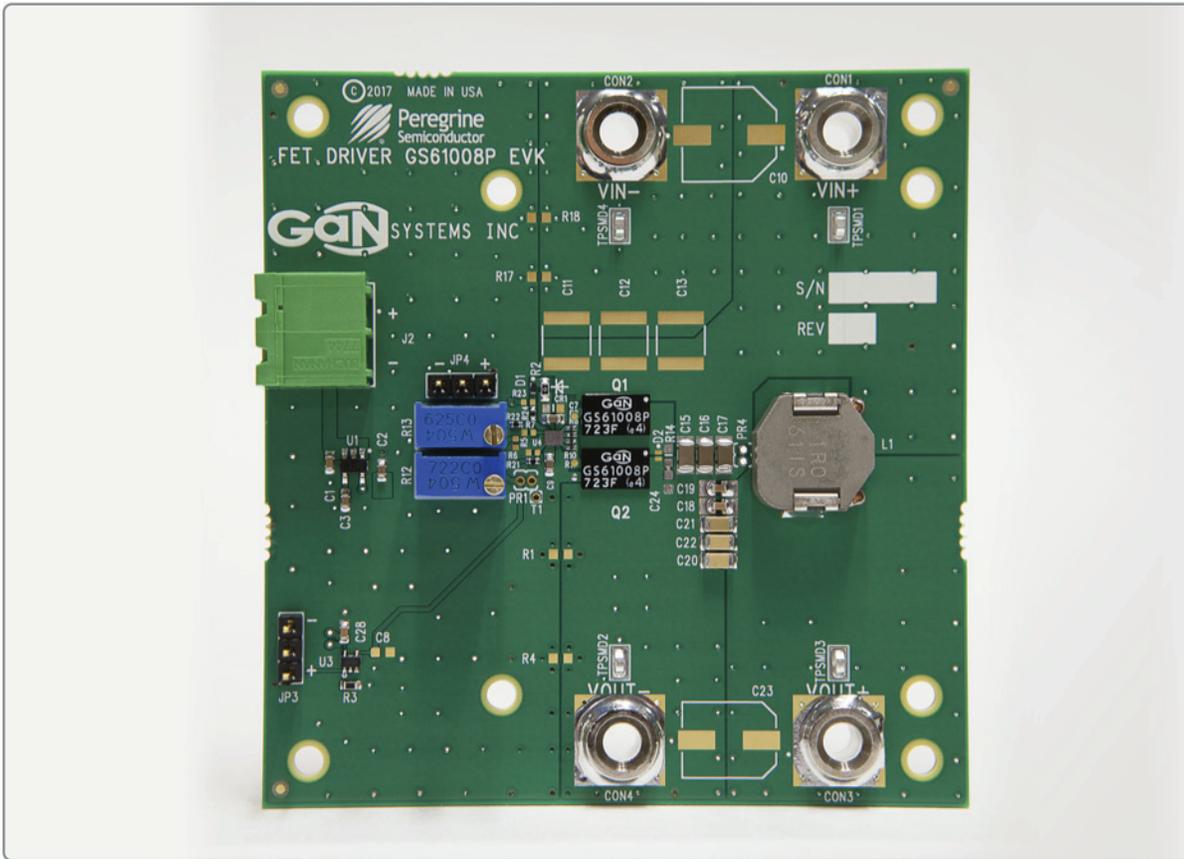


Figure 6 ■ Half-Bridge Driver Schematic

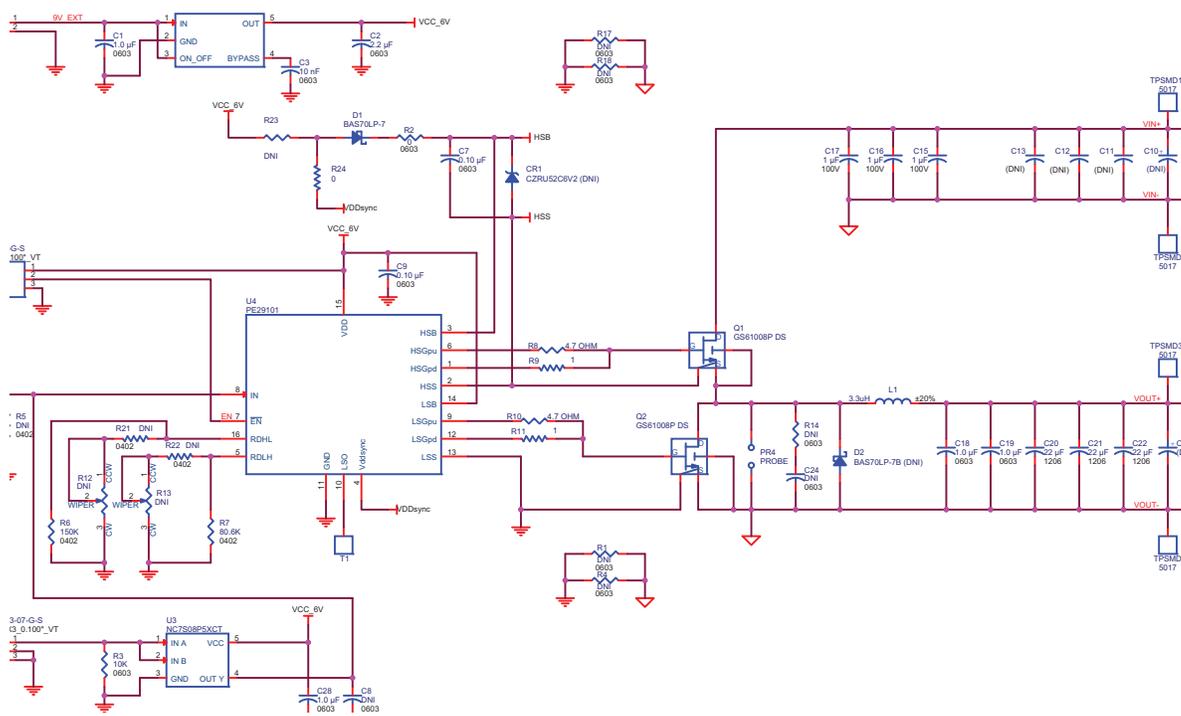


Figure 7 ■ Half-Bridge Driver Efficiency ($V_{IN}=48V$, $V_{OUT}=12V$, $FSW=1\text{ MHz}$)

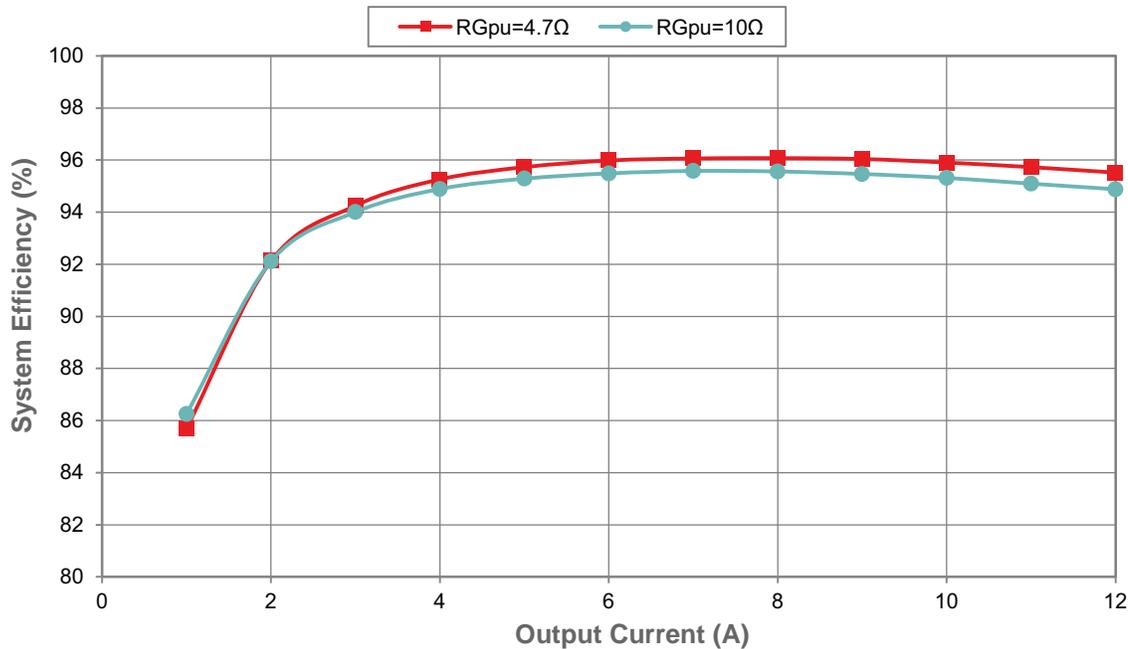
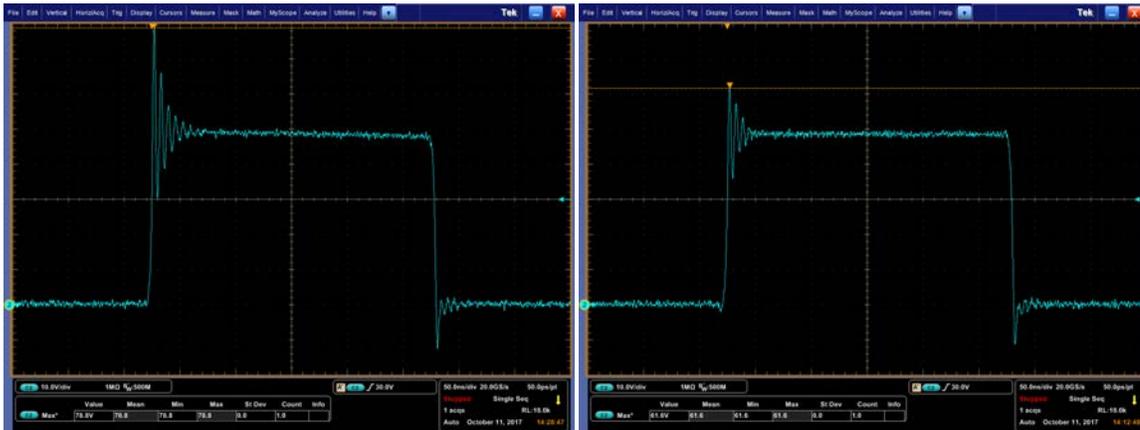


Figure 8 ■ Half-Bridge Driver Switching Waveforms at 10A Load With (a) 4.7Ω Gate Pull-Up Resistors and (b) 10Ω Pull-Up Resistor



Gate Driver Example 2

Figure 9 shows a development board using a PE29102 gate driver with a 30V EPC2111 eGaN® (Enhancement-mode Gallium Nitride) integrated circuit. The EPC9086 is a high-efficiency half-bridge development board that can operate up to 10 MHz. The development board has been evaluated in a 12V to point-of-load DC–DC converter application and achieved efficiency levels of 86% at 10A when switching at 5 MHz and over 80% when switching at 10 MHz (**Figure 10**)¹.

1.EPC9086 Quick Start Guide, Efficient Power Conversion Corporation, 2017.

Figure 9 ■ EPC9086 Half-bridge Development Board (Courtesy of Efficient Power Corporation)

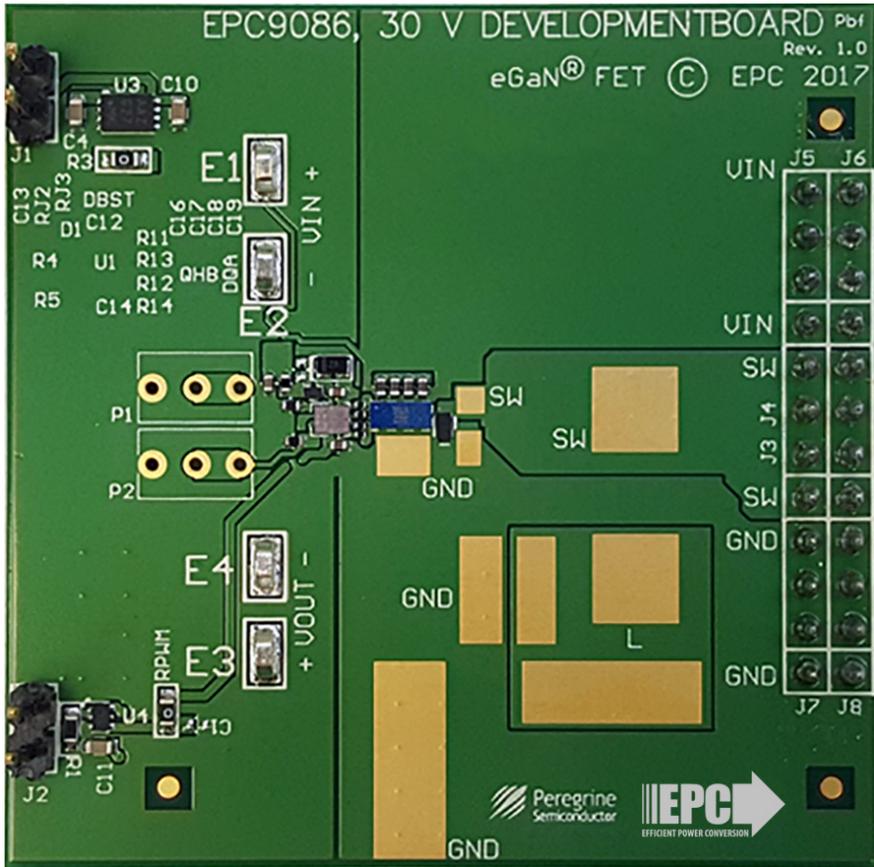
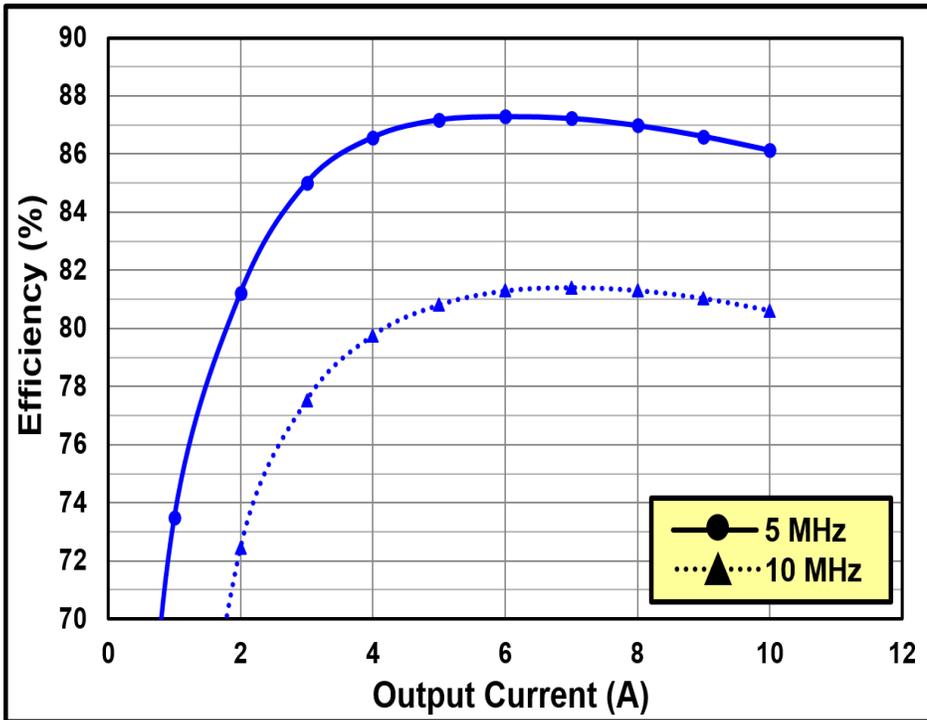


Figure 10 ■ Typical System Efficiency for $V_{IN} = 12V$ to $1.8V_{OUT}$ Buck Converter (Courtesy of Efficient Power Corporation)



Gate Driver Example 3

Figure 11 shows a class D audio amplifier reference design using two PE29102 gate drivers and four GS61004B 100V E-mode GaN transistors¹ in a full-bridge configuration. The reference board schematic is shown in Figure 12.

The input signal is fed into a logic-level buffer, U9. U5 is an exclusive or (XOR) circuit that coherently splits the phase of the input signal to the separate pulse-width modulation (PWM) inputs of U6 and U8 high-speed integrated gate drivers. The PE29102 drivers also include a phase control pin that determines which dead-time signal is fed to the high-side and low-side driver outputs. The dead-time resistors only affect the rising edge of the LSG and HSG outputs. Dead-time resistors RDLH (R51 and R53) will delay the rising edge of HSG, thus providing the desired dead time between LSG falling and HSG rising. Likewise, dead-time resistors RDHL (R52 and R54) will delay the rising edge of LSG, thus providing the desired dead time between HSG falling and LSG rising.

This full-bridge circuit may also be configured as two separate half-bridges. However, if two different signal paths are required throughout (as in stereo), then the two separate digital PWM input signals should be applied to the relevant test points TP1 and TP2 and the jumper pins removed from J200 and J3 to bypass U9 and avoid clashes with U5 outputs.

Both half-bridges that comprise the full bridge are protected by a common over-current detection circuit that sense high-side current draw through either or both power transistor paths to ground in the event of shoot-through or a short-circuit.

The 100W / 8Ω Class D audio reference design demonstrated >90% efficiency switching at 384 kHz.

Figure 11 ▪ Full-Bridge Class D Audio Amplifier Reference Design



1. GS61004B datasheet, <http://www.gansystems.com/gs61004b.php>

Figure 12 ■ Full-Bridge Class D Audio Amplifier Schematic

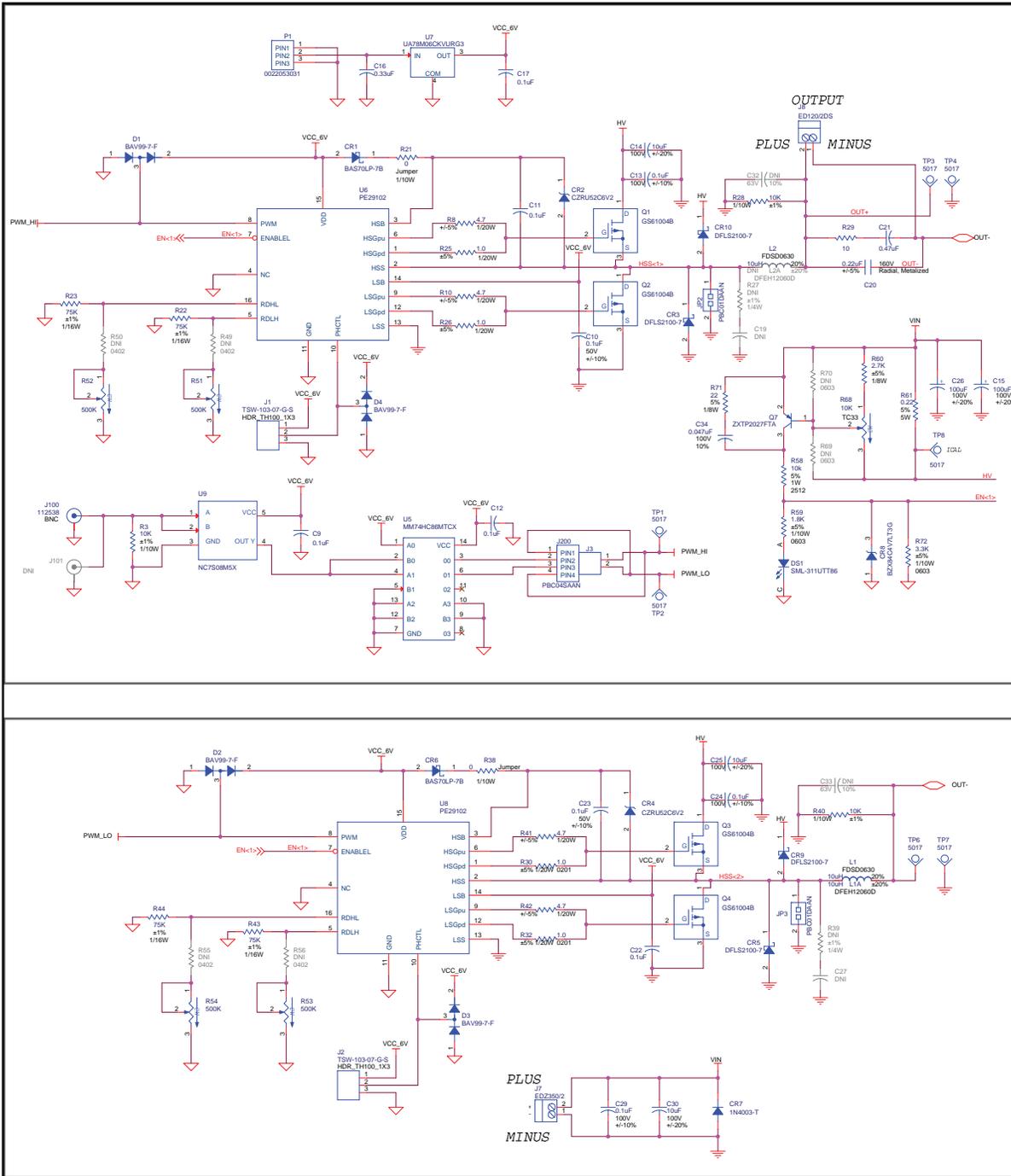
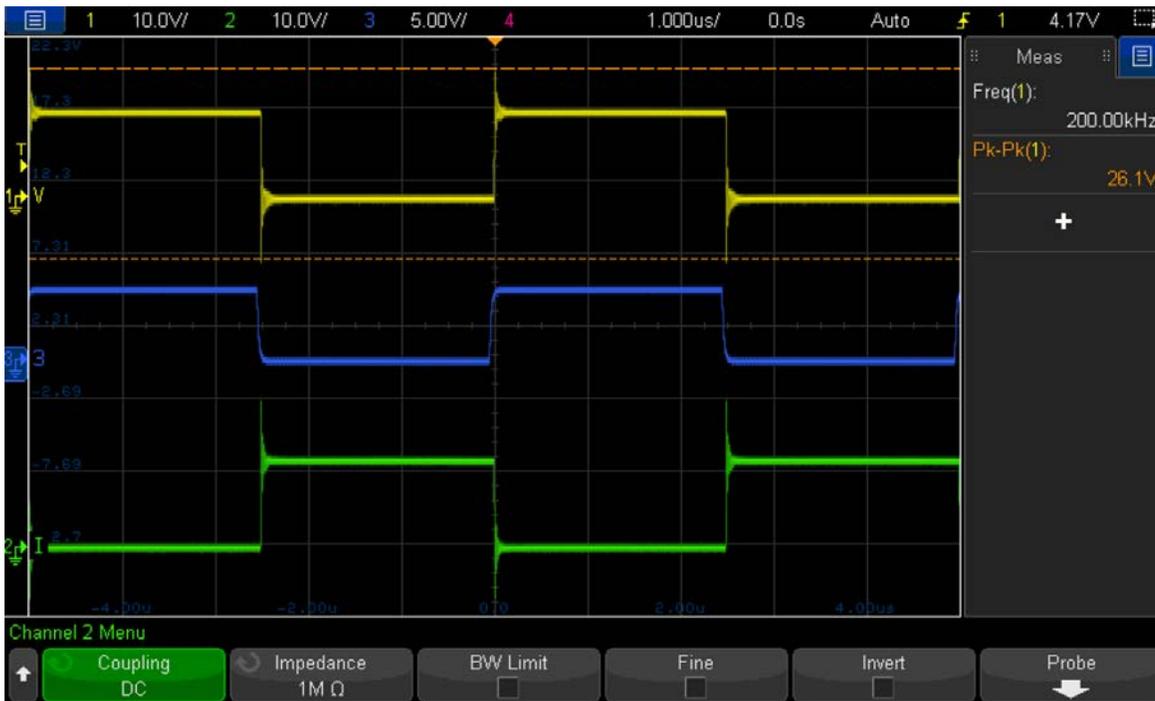


Figure 13 ■ Full-Bridge Class D Audio Amplifier Showing Both Switching Waveforms (Center Trace Shows PWM Input Signal at 200 kHz)



PCB Layout Considerations

High-speed switching applications require a PCB layout with low parasitic inductance. As the inductance increases, so does the peak voltage and ringing. **Figure 14** shows the gate loops in red and the power loop in blue. Excessive inductance in the gate loop can drive the gate voltage beyond the maximum rating of the GaN device. Excessive inductance in the power loop can cause undesirable ringing at the half bridge output and drive the drain voltage beyond the rated maximum. Common source inductances designated in green can result in parasitic oscillations reducing gate drive stability and switching speed. It is important to Kelvin sense the source terminal of the GaN device to avoid the common source inductance (more on this below). The parasitic loops shown in **Figure 14** become more prevalent as switching frequency increases.

Figure 14 ■ Schematic Diagram Showing PCB Parasitic Loops from Example 1

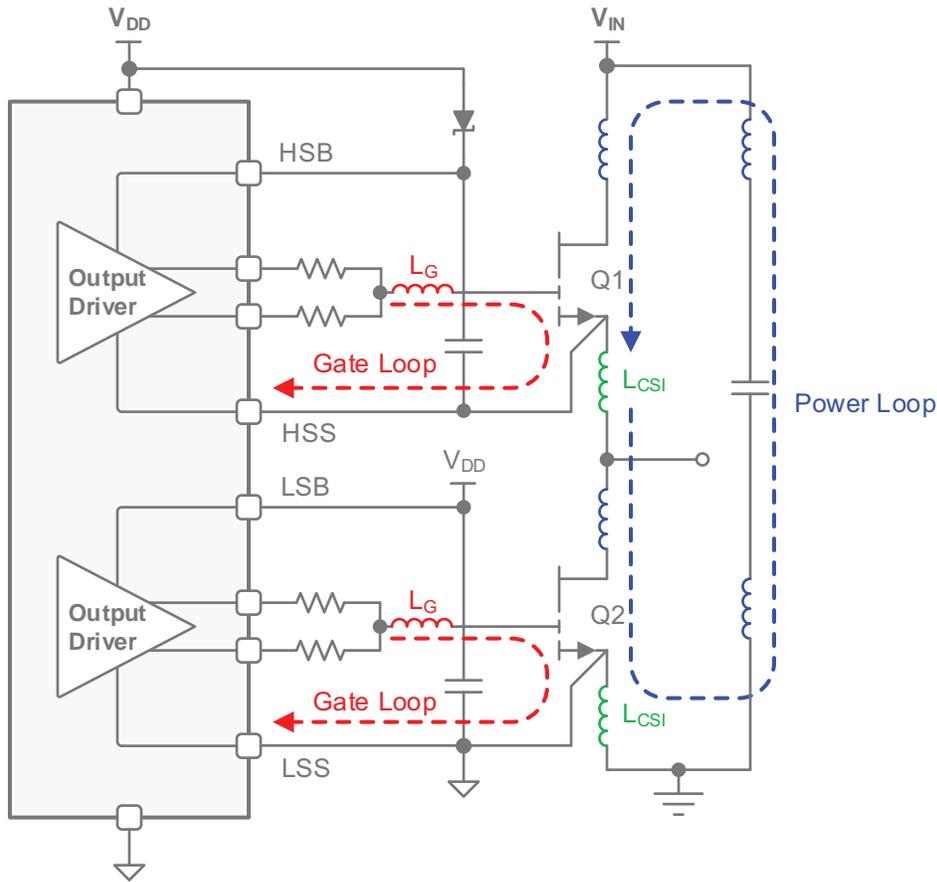
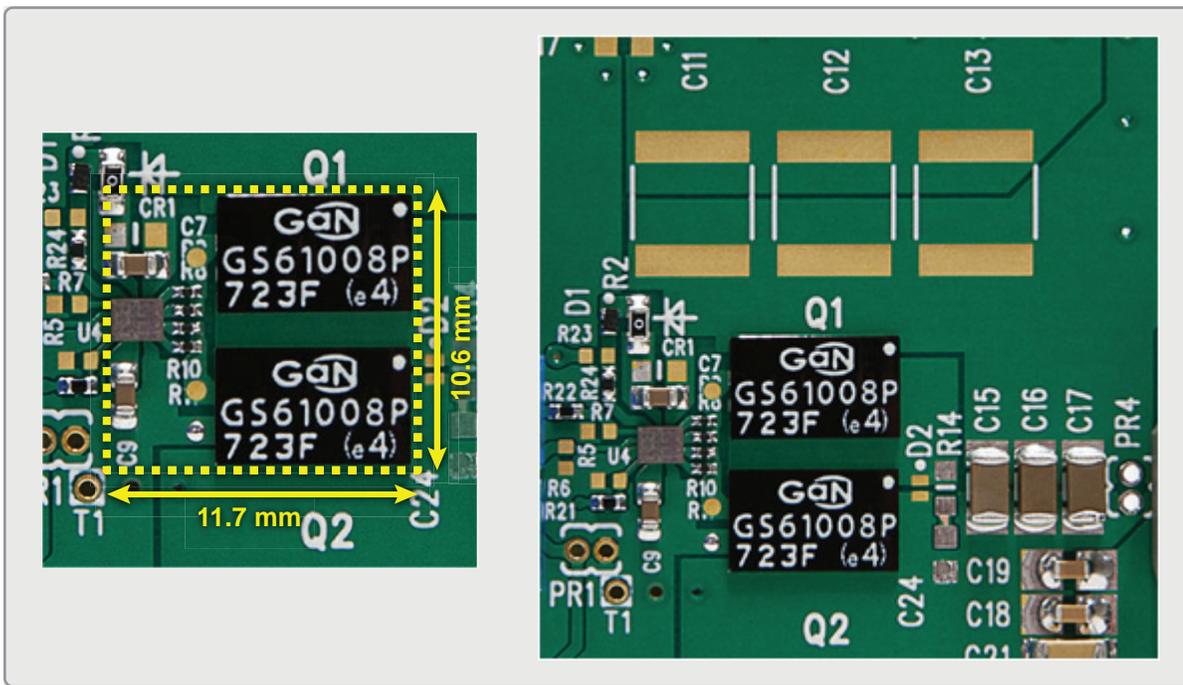


Figure 15 shows the critical layout section of the top side of the gate driver used in Example 1. The small 0201 surface mount gate resistors allow the driver (U4) to be placed close to the transistors to minimize the gate loop inductance. The gate driver ground plane is referenced to the source sense pad (also called the gate return pad) of Q1 and Q2. For transistors that do not have a dedicated gate return pad, it is important to Kelvin connect the gate return route as close as possible to the source pad of the transistor and separate the gate return route from the high current power path of the source terminal. This will minimize or eliminate the effect of the common source inductances on the gate drive signals. It is recommended that the gate return route down to the second layer of PCB through vias and route back to the gate driver underneath the gate resistors in order to take advantage of magnetic coupling cancellation within the gate loop. The spacing between the layers that route the gate loop should be small (5–8 mils typically), but must be able to handle high voltage if applicable. Bypass capacitor (C9) and bootstrap capacitor (C7) are placed close to the driver to reduce noise coupling.

The power loop inductance is reduced by placing bypass capacitors C15–C17 (and optionally C11–C13) close to Q1 and Q2. The power return path from the source pad of Q2 should take the shortest possible path back to

C15–C17. The gate return path should be separated from the power return path, even though both paths may be sharing the same nodes or pads.

Figure 15 ■ Gate Driver Example 1 PCB Layout (Top Side)



Figures 16 through 19 show the critical areas of the PCB layout in “Gate Driver Example 1”.

Figure 16 ■ Top Layer

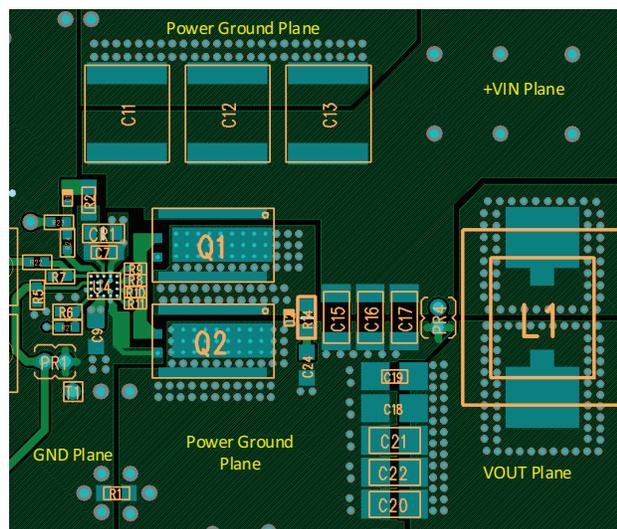


Figure 17 ■ Mid-Layer 1

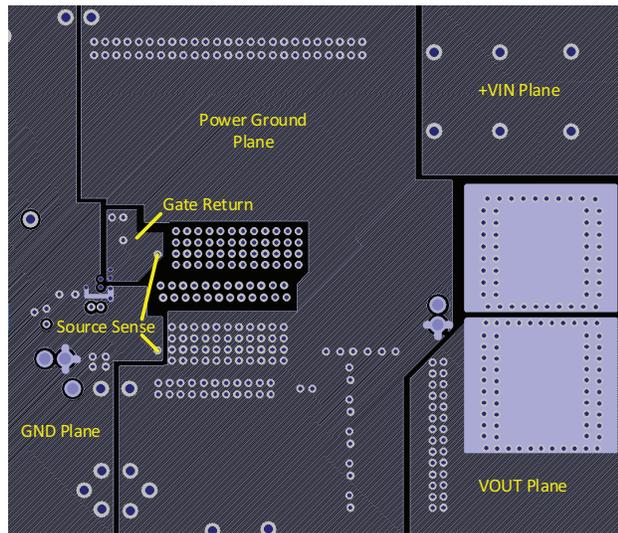


Figure 18 ■ Mid-Layer 2

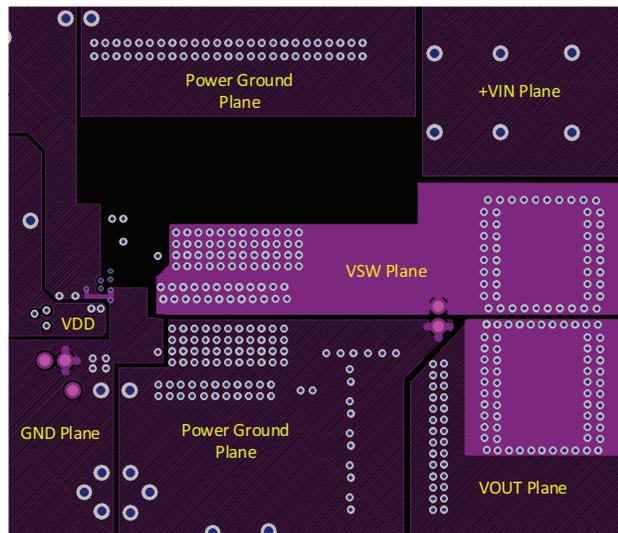
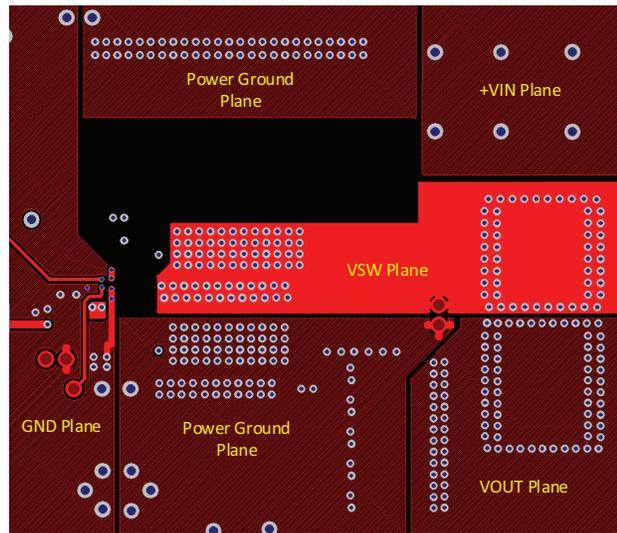


Figure 19 ■ Bottom Layer



Thermal Considerations

The thermal pad (substrate) of each transistor is connected to its source pad by a copper plane on the top layer and linked through multiple vertical interconnect access (via) holes to the bottom layer. Wide planes are used to provide thermal dissipation. A heatsink can be attached to the PCB underneath the thermal pad.

As load current and switching frequency increase, the thermal performance decreases. The addition of heat-sinking and/or forced air cooling can significantly increase the current rating of the gate driver circuit examples, but care must be taken to not exceed the absolute maximum junction temperature of the devices.

Conclusion

This application note has outlined gate driver design principles and layout techniques that should be considered when designing drive circuitry for enhancement-mode GaN transistors. Three reference design examples have been shown using Peregrine Semiconductor's high-speed gate drivers.

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