Using the PE29102 as a Power-up Sequencer for Depletion-mode RF GaN HEMT Amplifiers

Application Note 74

Summary

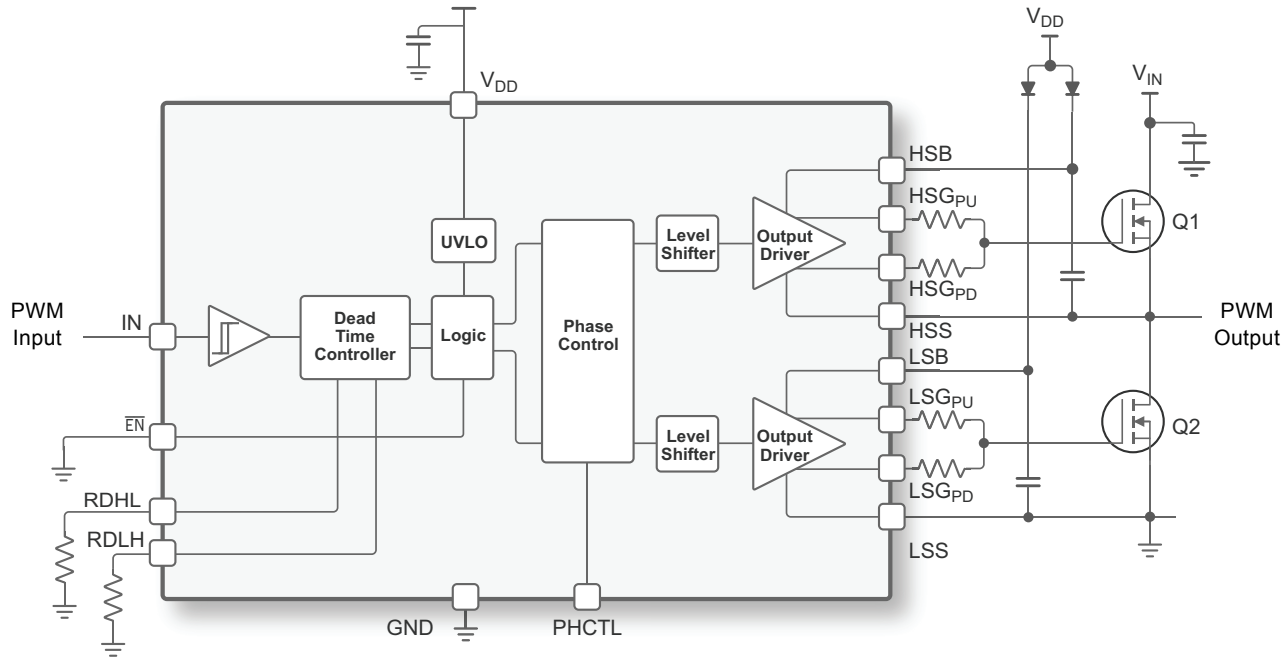
This application note outlines how the PE29102 pulse width modulation (PWM) gallium nitride (GaN) driver can be used as a power-up sequencer for use with depletion-mode GaN radio frequency (RF) transistors. It considers several suitable circuit configurations and determines which one presents the most advantageous use with a GaN power switch. The final circuit is a real implementation with a depletion-mode GaN amplifier device showing the correct power-up and power-down sequence.

Introduction

The PE29102 is a high frequency field-effect transistor (FET) driver designed for use in PWM-type power switching and Class D audio switching that can also be configured for other uses. This application note outlines the use of the PE29102 as power-up sequencer (PUS).

Figure 1 shows the basic configuration of the PE29102 application circuit.

Figure 1 ▪ Test Circuit for PE29102



The PE29102 has several features that make it flexible so that it can be configured for a PUS.

The device has a programmable output dead time. This means that the outputs, high-side gate (HSG) and low-side gate (LSG), are never high at the same time. In the original PWM application, this is used to prevent current rush-through between high side and low side switching FETs by preventing the FETs being turned on simultaneously.

The device gate output levels are also set externally through the high-side bias (HSB) and low-side bias (LSB), with the return connections through the high-side source (HSS) and low-side source (LSS).The high side and low side are isolated from one another and from the PE29102 device supply. This allows the outputs to be configured for various external FET configurations, with gate drive voltages of up to 60V allowed. In the example shown in **Figure 1**, the HSG output is connected as a bootstrap allowing the HSG to swing between 0V and the external FET drain voltage, VIN.

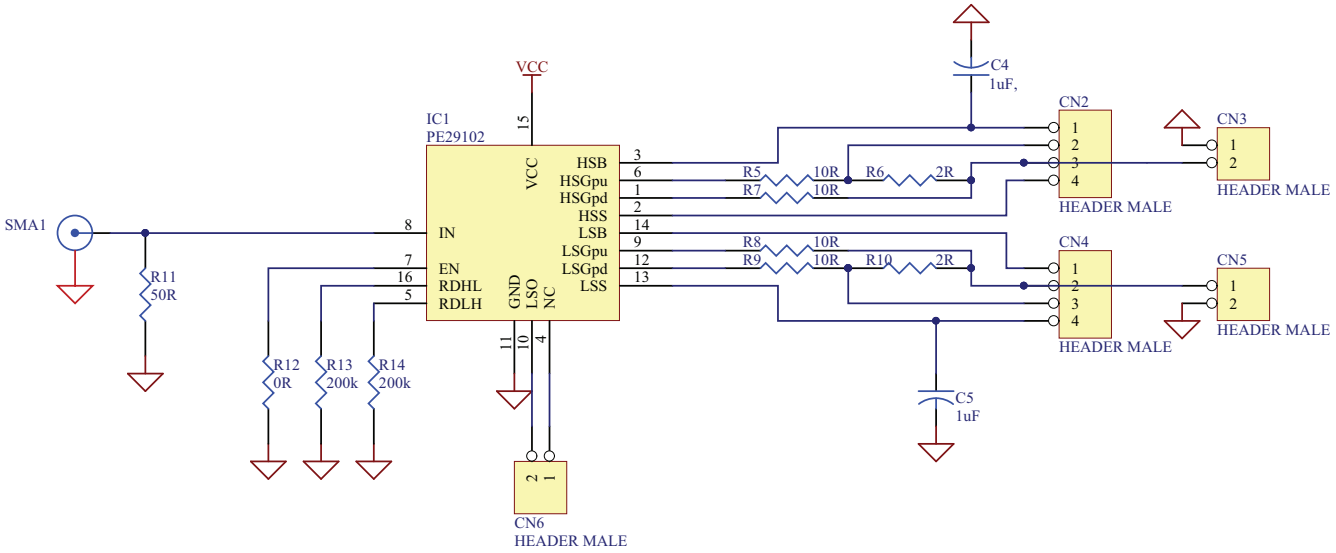
Bootstrap Function

The purpose of the capacitor connected between the HSB and HSS of the PE29102 is not immediately obvious. This is known as the bootstrap capacitor and is used to ensure that, when required, the HSG gate of the high side FET, Q1, stays above the HSS potential. Referring to **Figure 1**, the following description of the bootstrap function V_{DD} is assumed to be 5V and V_{IN} is 60V.

When you apply the enable pulse to the PE29102 PWM input, the HSG gate drive rises through the diode to the HSB input level. This is 5V, assuming no diode drop. But as the Q1 turns on, the Q1 source rises to V_{IN}, ~ 60V, and the bootstrap capacitor allows the HSB and hence HSG to follow, staying above the Vs (60V) by the original HSB voltage (5V). This ensures that the HSG rises to 60+5V to maintain the positive gate voltage above the Q1 source voltage. Note that as the V_{DD} diode is no longer conducting to charge the capacitor, the HSB and hence HSG will eventually drop back to 60V depending on capacitor value and the gate leakage current. This means this configuration can only be used for a pulsed system rather than a system with constant offset voltage.

Figure 2 shows a more basic configuration for the PE29102.

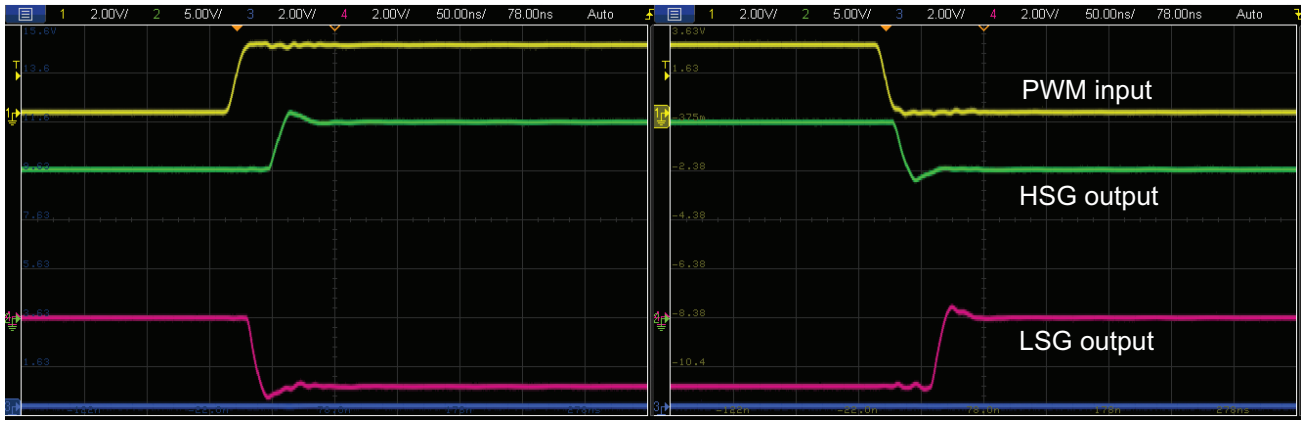
Figure 2 ▪ Basic Circuit Configuration for the PE29102 without the Bootstrap Function



The HSG and LSG outputs are still the drivers to the gates of external switching FETS through the headers CN1 and CN4. The voltage out high (Voh) and voltage out low (Vol) levels for these signals are defined by the HSB and HSS, and the LSB and LSS inputs, respectively. The HSG and LSG outputs are isolated, allowing one output to be set for a positive bias voltage and the other to be set for a negative bias voltage.

With the PE29102 dead time function, the positive-going HSB pulse output always lies within the LSB negative-going pulse, as shown in **Figure 3**. These features make the PE29102 ideal for use when undertaking a power-up sequence for a depletion-mode device such as an RF GaN high electron mobility transistor (HEMT).

Figure 3 ▪ Gate Bias Sequence



RF GaN Bias Requirements

RF GaN devices are mostly depletion-mode HEMT devices that require a negative gate voltage. This must be applied before any drain voltage is applied. The gate voltage is needed to pinch off the device so that there is no current rush through the device when the drain voltage is applied. Applying any drain voltage before the gate bias would destroy the device. Because these are depletion devices, the required gate bias is negative. Normally, a negative voltage generator would be generated from the same supplies used to drive the device V_{DD}. This makes it difficult to generate the required RF GaN FET negative gate bias voltage before the RF GaN drain voltage (V_{DD}) is applied. Therefore, some kind of RF GaN FET V_{DD} switch is required along with a gate bias sequencer. The PE29102 provides the ability to handle negative gate voltages while also providing the correct power-up sequence. **Figure 3** shows a typical sequence that can be achieved. The yellow line represents the sequence enable signal. The green and red lines represent the HSG and LSG outputs. These become the V_{DD} switch gate voltage and the RF GaN HEMT gate voltage, respectively. Note that the negative-going red line signal stays outside of the positive-going green line signal. This would ensure the RF amplifier negative gate voltage is present for the whole time the positive gate is present.

Power Supply Sequencing Configurations

Several configurations can be used to implement the power-up sequence using a V_{DD} switch. Three configurations are outlined in this application note, with some notes to define the advantages and disadvantages of each configuration. The three configurations are:

- Ground switching
- V_{DD} switching
- PMOS V_{DD} switching FET

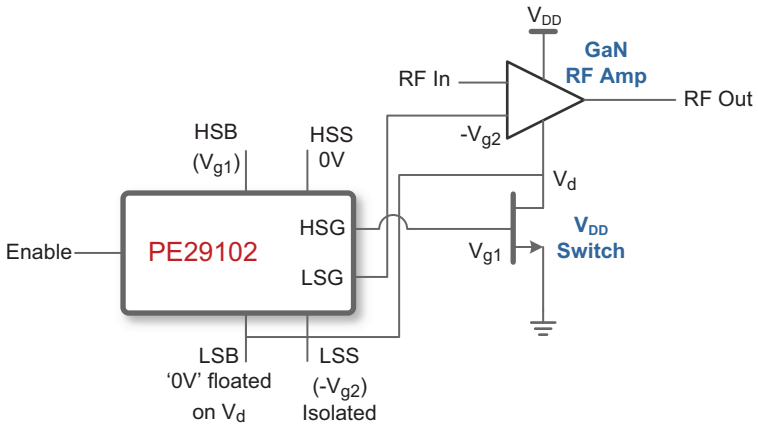
Configuration 1: Ground Switching

For an overview of this configuration, see **Figure 4**.

This is the easiest to implement when considering the V_{DD} switch and PE29102 controller.

The V_{DD} switch gate bias,Vg1, is applied to HSB and HSS. The negative gate bias for the RF amplifier (-Vg2) is applied across LSB and LSS. Vg2 must be floated upon the V_{DD} switch drain voltage (Vd), but this is simply achieved by adding a bootstrap connection between the V_{DD} switch Vd and LSB with an isolated DC-to-DC supply to provide the LSB and LSS supply.

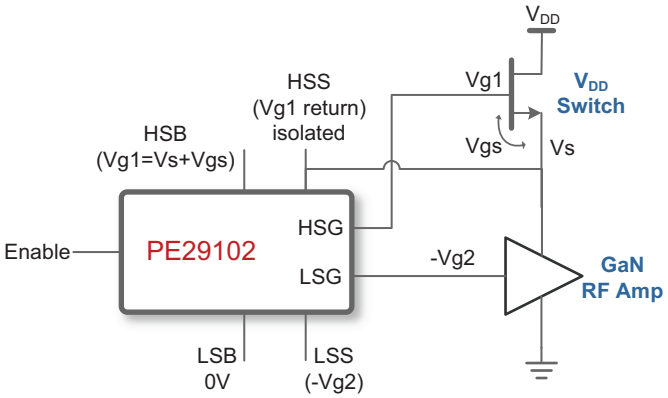
Figure 4 ▪ Ground Switching V_{DD}



Configuration 2: V_{DD} Switching

In this configuration, to bias the V_{DD} switch correctly requires Vg1 to be floated upon the V_{DD} switch source voltage (Vs) by the required FET Vgs. This cannot be achieved with a bootstrap capacitor as the duty period is undefined and could be longer than the bootstrap time constant. The supply to HSB and HSS needs to be isolated from the remainder of the circuit so that it can be floated on the V_{DD} switch FET source voltage Vs. This means the Vg1 will swing between ~ 0V and V_{DD} + Vg1. As -Vg2 for the RF amplifier is referenced to the circuit 0V, it can be supplied by any external negative voltage present elsewhere, or provided by an isolated Vg supply as before. **Figure 5** shows an example of a switched V_{DD} configuration.

Figure 5 ▪ Switched V_{DD} Configuration

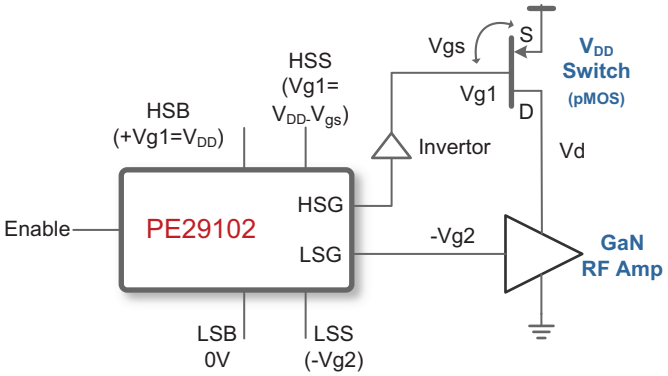


Configuration 3: PMOS V_{DD} Switching FET

Figure 6 shows the most standard configuration for V_{DD} switching. It allows the Vgs of the positive channel metal oxide semiconductor (PMOS) to swing between 0 and 5V (Vg1 swings between V_{DD} and V_{DD}-Vgs) while allowing the Vd to rise and fall between V_{DD} and 0V without the risk of damaging the FET. The device must be selected to have Vds breakdown greater than the V_{DD} being used.

In this case, however, the PE29102 HSG output is a positive-going pulse but a PMOS device requires a negative-going pulse. This means the HSG output has to be inverted while operating between V_{DD} and V_{DD} - Vgs. This makes this configuration with the PE29102 too difficult to implement and offers little advantage over a standard PMOS circuit.

Figure 6 ▪ PMOS Switched V_{DD} Configuration



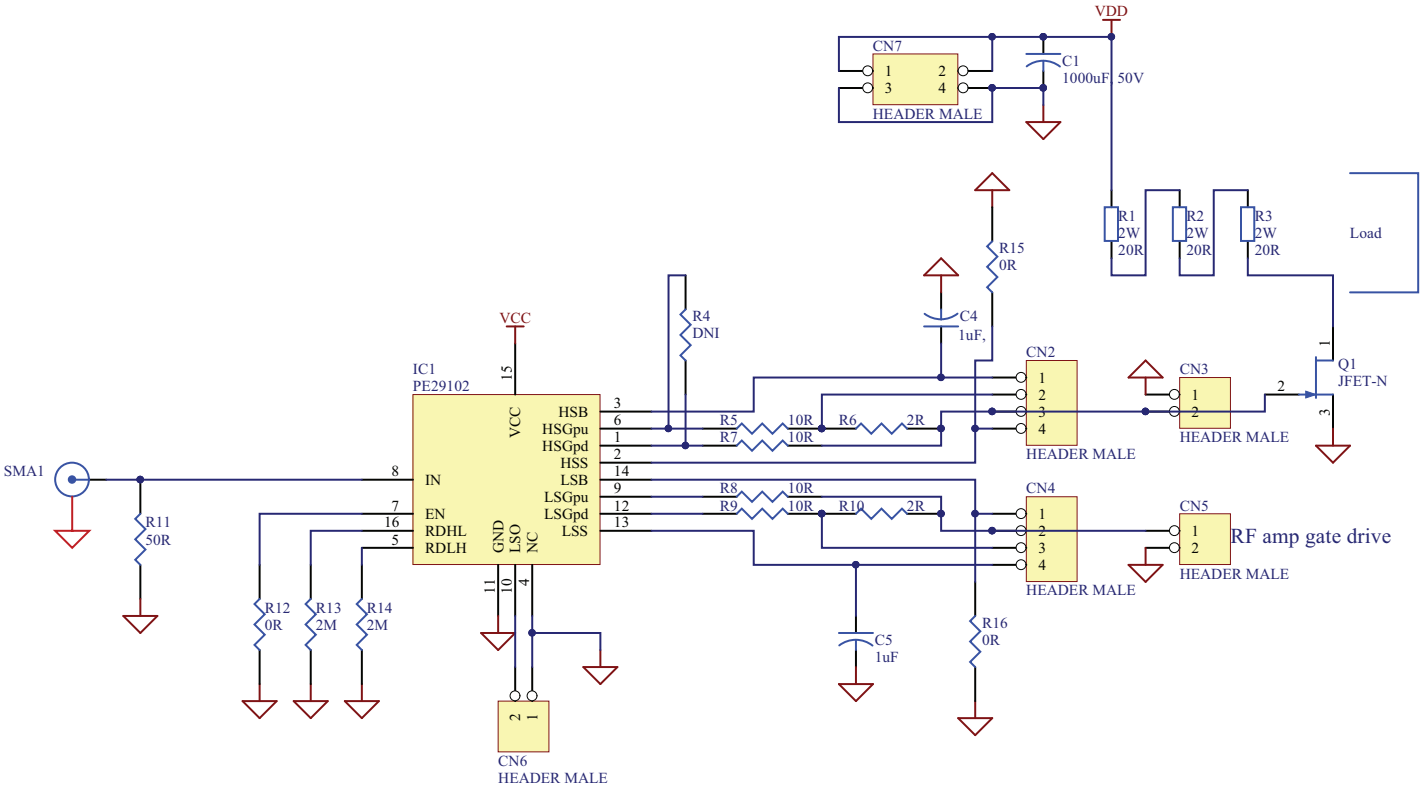
Circuit Evaluation

Until now, we have considered only the basic circuit configurations. In this section, we implement and test the switched V_{DD} and switched ground configurations, and identify the additional circuit requirements needed to realize a real circuit. For the switched V_{DD} configuration, we show the performance of the circuit when driving a real depletion-mode RF GaN amplifier.

Configuration 1: Ground Switched V_{DD} Circuit

Figure 7 shows the evaluation circuit used to demonstrate this capability using the ground switched configuration (as shown in **Figure 4** on page 5). The Q1 V_{DD} switch is a GaN Systems GS61004B. This is an example device, but any suitable GaN switch that has sufficient current and voltage limits that meet the RF amplifier requirements and is within the PE29102 80V limit can be used.The RF GaN PHEMT is represented by the load resistors with the negative gate drive being the PE29102 LSG output. V_{DD} is set to 24 V, HSB is set to 5V, and LSS is set to -5V.

Figure 7 ▪ Schematic Implementation



The resultant control signals are shown in **Figure 8** and **Figure 9**.

Figure 8 ▪ Switched Ground Signals

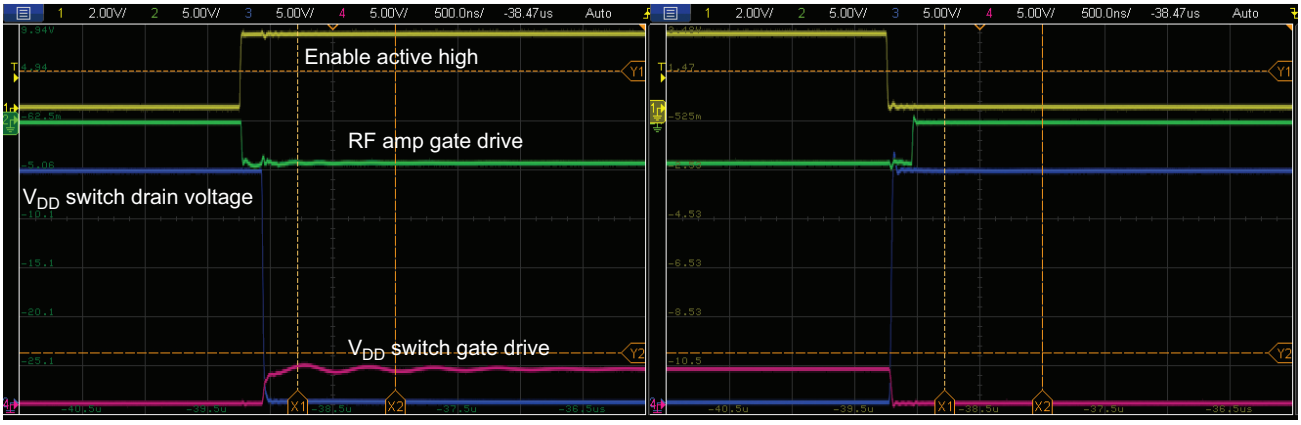
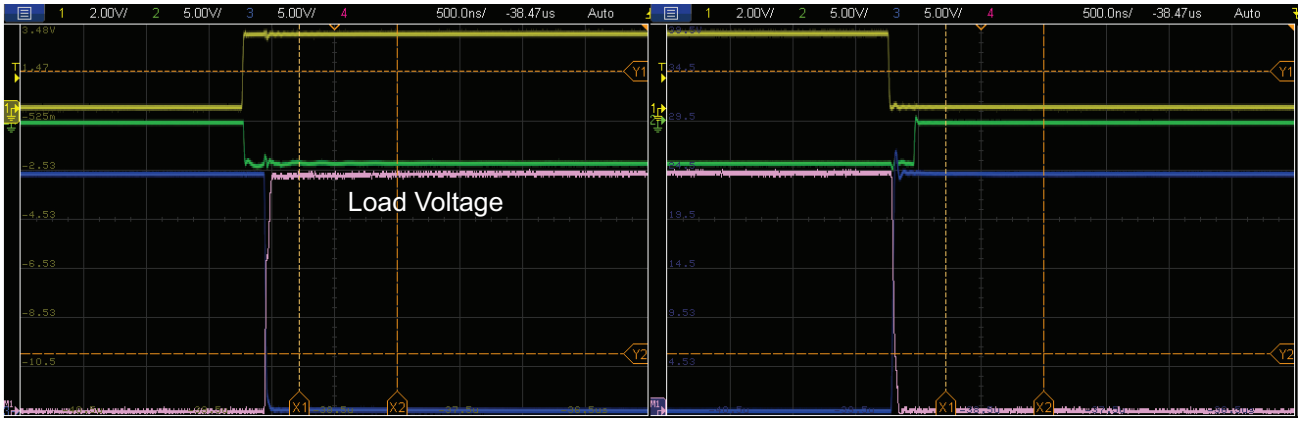


Figure 9 ▪ Same Traces as Figure 8 but Now Showing Voltage Across the Load



For power-up, the PE29102 controls the power-up sequence by applying the RF FET negative -3V gate voltage before the 24V load voltage.

For power-down, the PE29102 controls the power-down sequence by removing the load voltage before the RF FET gate voltage.

However, this only shows proof of concept. It is a simplified implementation and neglects to show the LSB bootstrap. If this circuit was implemented, the Vgs of the RF amplifier would be exceeded and the amplifier would be destroyed.

'DC Bootstrapping' the Switched Ground Circuit

The outputs of the PE29102 are isolated. This allows the outputs to be floated on whatever voltage is needed, provided the following conditions are met: The maximum allowed voltage potential between the HSB and HSS or the LSB and LSS nodes must not exceed 7V, and the difference between the HSG and LSG outputs must not exceed 60V.

Figure 8 and **Figure 9** show the functionality of the switched ground circuit, but they do not address the detail of the Vg for a real load (in other words, the RF amplifier). The source voltage of the RF amplifier will vary between ground and approximately V_{DD}. This means that the gate voltage of the RF amplifier must follow this voltage, and so a bootstrap connection must be added to the circuit. This is shown in **Figure 10**. The LSB supply for the RF amplifier is floated upon the V_{DD} switch FET Q1 drain voltage Vd. This means an isolated DC-to-DC converter must provide the LSB and LSS voltages. Such a device is a Murata CME or LME device, as shown in **Figure 11** on page 11.

An added complication exists in this configuration represented by the RF ground capacitor shown in **Figure 10**. The RF amplifier source is not the circuit RF ground, and this point must be adequately RF decoupled to the RF ground of the surrounding circuit. Failure to do so could compromise the RF amplifier performance.

Circuit Implementation: Switched Ground

Figure 10 ▪ Block Diagram Showing a DC 'Bootstrap' Connection

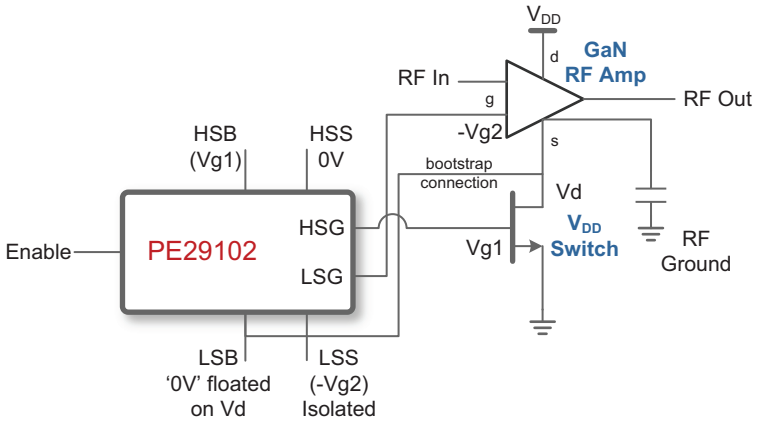


Figure 11 ▪ Schematic of the Circuit Implementation

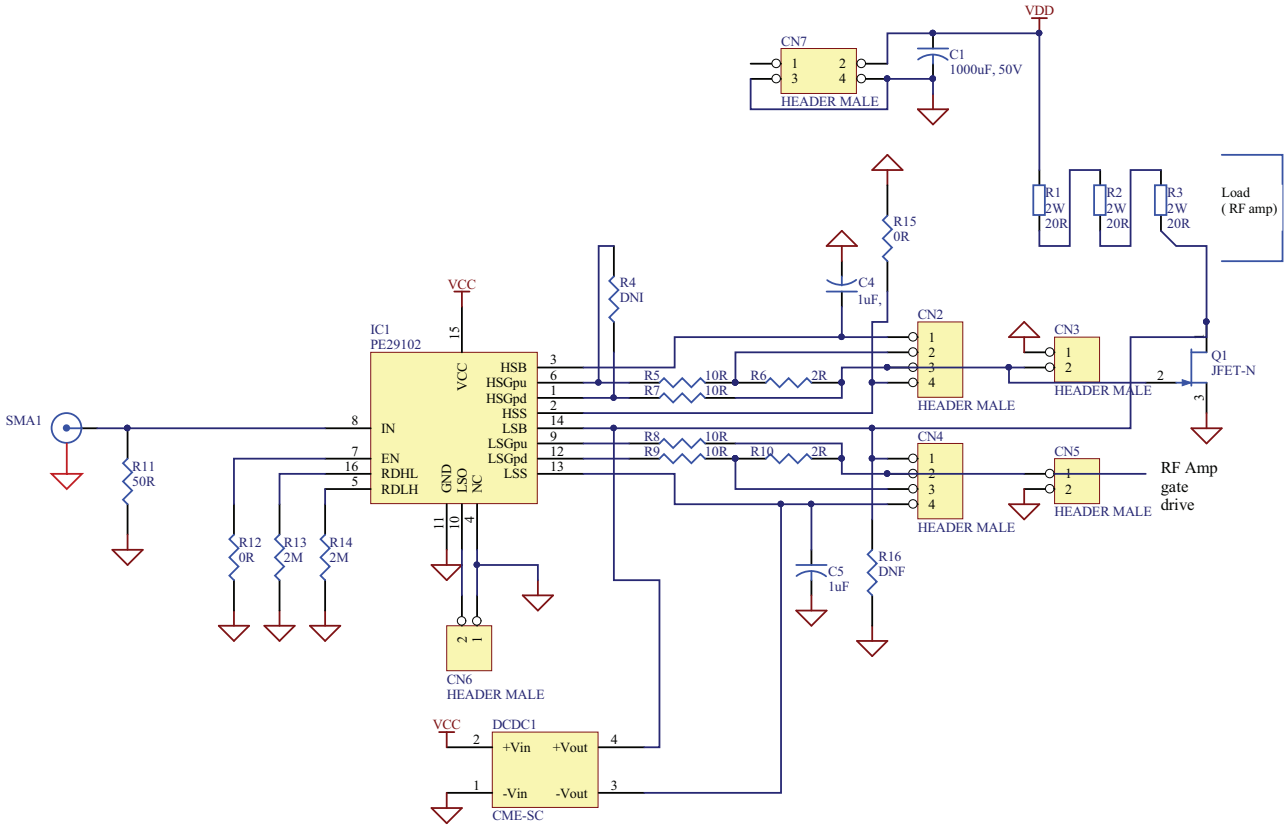
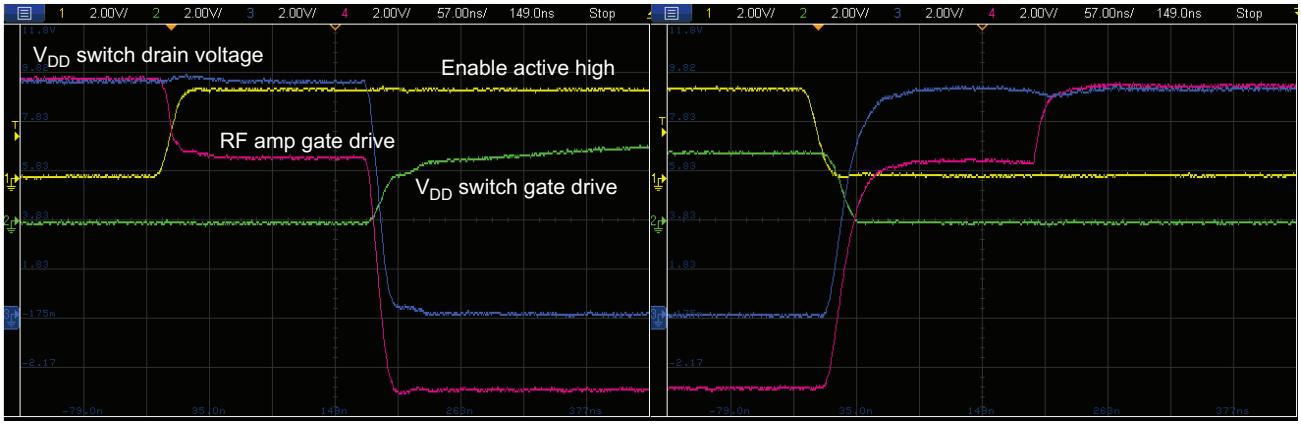


Figure 12 shows the voltage traces showing the circuit operation with the bootstrap function.

Figure 12 ▪ Switched Ground Signal with the Bootstrap



Circuit Operation

Before enable is applied, the load (RF amp) Vs and Vg are both at V_{DD}. However, although the RF amp is depletion mode, no current flows through the RF amp as the V_{DD} switch/Q1 is pinched off. This is because the V_{DD} switch gate drive, Vg1, is 0V. When enable is applied, LSG becomes the value of LSS and the load (RF amp) Vg drops below V_{DD} by the LSS node voltage. This will bias the RF amplifier. After the time defined by the PE29102 dead time, HSG becomes the value applied to HSB. This opens Q1/V_{DD} switch, and current flows through the RF amp as defined by the bias point of the RF amplifier. Note that LSG tracks the drop of Q1/V_{DD} switch Vd while maintaining the negative operating bias.

When enable is removed, HSG becomes the HSS voltage or 0V, and Q1/V_{DD} switch pinches off. The RF amp gate bias rises with Q1/V_{DD} switch Vd but maintains the negative bias. After the dead time, LSG becomes LSB or Vd removing the negative bias to the RF amplifier.

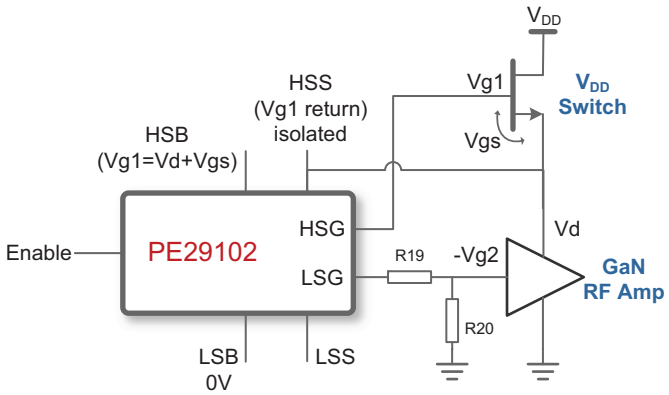
As stated earlier, there is one major disadvantage to the switched ground circuit: The ground of the RF amplifier is not 0V. This means that the RF amplifier will need RF decoupling to the 0V / ground of any external RF circuit.

Due to the difficulties with the RF amplifier ground isolation, this circuit has not been tested with an active RF amplifier.

Configuration 2: Switched V_{DD}

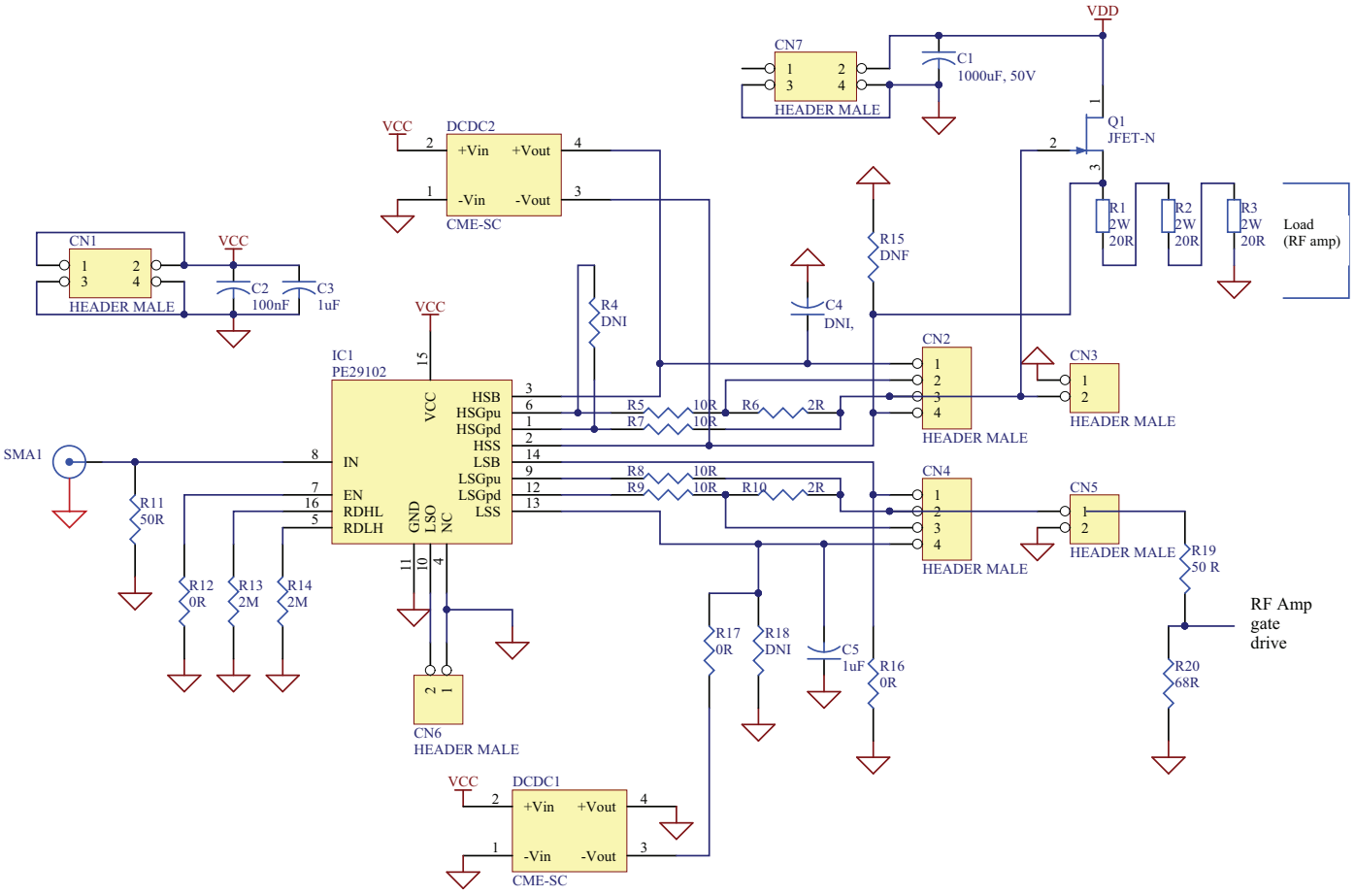
This circuit implementation would seem the most obvious to use. See **Figure 13**. It is easier to implement, because the RF amplifier ground is the same as the power ground.However, it still requires Vg1 to track the Vd of the RF amplifier using a similar bootstrap connection as in Configuration 1.

Figure 13 ▪ Switched V_{DD} Configuration



The voltage Vg1 is less critical, because the bias of the V_{DD} switch bias is less sensitive, so it is simple to provide an isolated supply for HSB and HSS. The RF amplifier gate bias, Vg2, is a negative voltage and if this is not available externally, then another isolated DC-to-DC converter will be needed to generate this negative voltage. Note that the minimum allowed voltage potential between the PE29102 HSB and HSS and the LSB and LSS input is 4V. If either Vg1 or Vg2 requirement is less than this, it must be provided by a potential divider on the HSG or LSG output(s). This is implemented using R19 and R20 in the circuit below. **Figure 14** shows the circuit schematic.

Figure 14 ▪ Switched V_{DD} Schematic

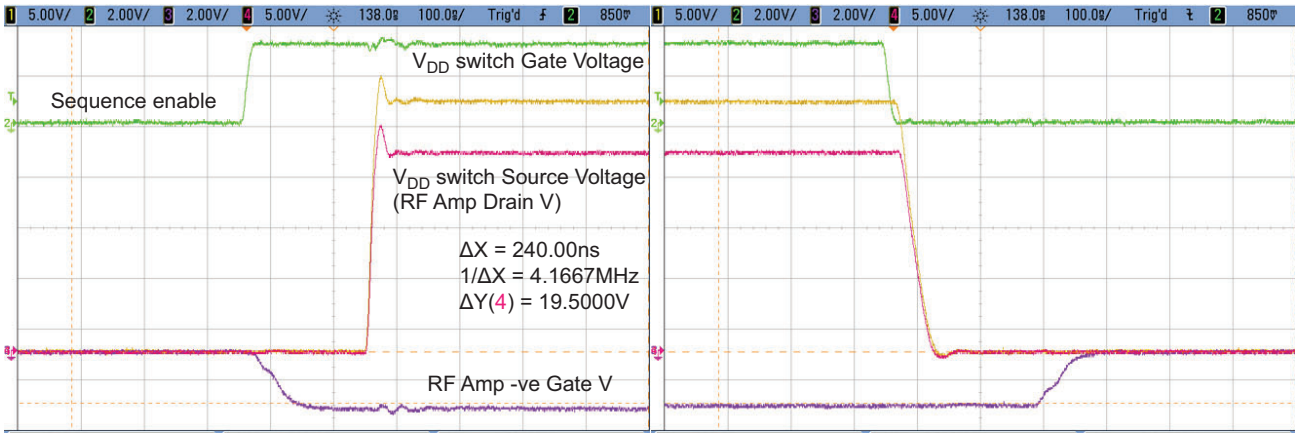


Switched V_{DD} Function

Refer to **Figure 14** and **Figure 15** on page 14. When the sequence enable signal is applied, the LSS input voltage becomes the negative gate bias, LSG, for the load (RF amp). The HSG output then rises to bias the V_{DD} switch. When HSG rises, the gate for the Q1/V_{DD} switch is applied, and it starts to conduct. The bootstrap connection to HSS ensures HSG/Vg1 rises with 'Load' voltage to ensure Vgs remains positive with regard to the Q1/V_{DD} switch source voltage.

For power-down, the HSG output drops, turning the Q1/V_{DD} switch off. The load/RF amplifier Vd then falls as the load V_{DD} is removed. HSG drops with it. The PE29102 LSG output to the RF amp gate voltage Vg2 is then removed after the PE29102 dead time.

Figure 15 ▪ Switched V_{DD} Power-up/Power-down Sequence



Using the Switched V_{DD} Circuit with a Real Depletion Mode GaN HEMT RF Amplifier as the load

The circuit shown in **Figure 14** on page 13 can then be used to apply a correctly-sequenced power-up sequence to a depletion-mode GaN amplifier. In this case, a wide band amplifier is used which is based upon a Cree 40006S transistor. This transistor requires a negative gate bias voltage of ~ -2.7V with a drain supply of 10 to 24V. The -2.7V is generated from the 5V LSG with an external potential divider. This should give a device current draw of ~100 mA. The amplifier replaces the 60 Ohm dummy load in the original circuit with the C40006S gate, connected to the PE29102 LSG output via R19 and R20.

It is important to remove any large supply decoupling capacitors on the amplifier evaluation kit. These would prevent the gate or drain from rising and falling in the required time defined by the PE29102 dead time. Any large decoupling capacitors should be applied to the drain supply of the V_{DD} switch rather than the RF amplifier. This means the layout needs to be considered carefully, including any ground return current paths, to prevent any ringing on the bias circuits. **Figure 16** shows the RF output during the power-up and power-down sequence.

Figure 16 ▪ RF Output Pulse Resulting From the PE29102 Power-up and Power-down Sequence

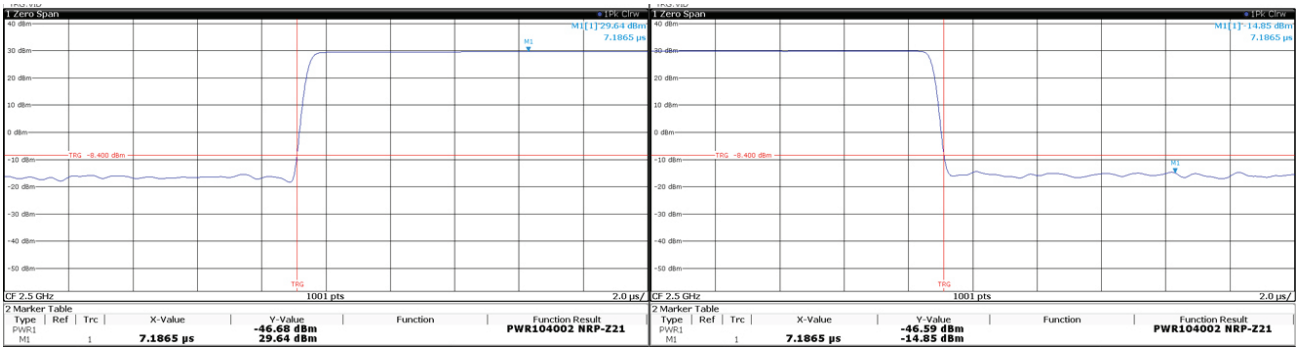
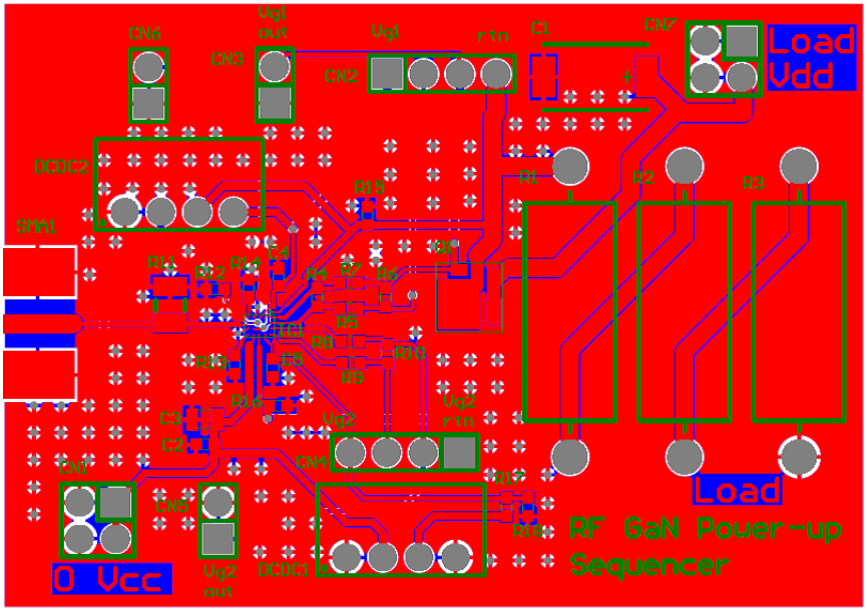


Figure 17 shows the sequencer board layout:

Figure 17 ▪ Sequencer Board Layout



Conclusion

The PE29102 has been successfully used to implement a depletion-mode GaN HEMT amplifier power supply sequencer.

The circuit provides the correct application of the GaN amplifier negative bias gate voltage before the drain voltage is applied. It also applies the correct power-down sequence as a reverse of the power-up sequence by removing the drain supply before the negative gate bias.

Sales Contact

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