

# PE29101/102 Footprint Requirements

*Application Note 77*



## Summary

This application note shows an example of a PE29101/102 footprint that uses a larger pad size. This eases the assembly of the chip-scale package (CSP) to a high-power circuit board that requires a thicker copper layer.

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## Introduction

The PE29101/102 devices are supplied in a chip-scale, flip-chip package. This application note outlines the use of oversized solder pads, which is important for the manufacture of high power circuits that use a thicker copper layer for improved current conduction and heat dissipation.

The data sheet specifies a 90  $\mu\text{m}$  diameter footprint pad. This specification often causes concern when the device is mounted upon a board which incorporates large power devices such as GaN switching transistors.

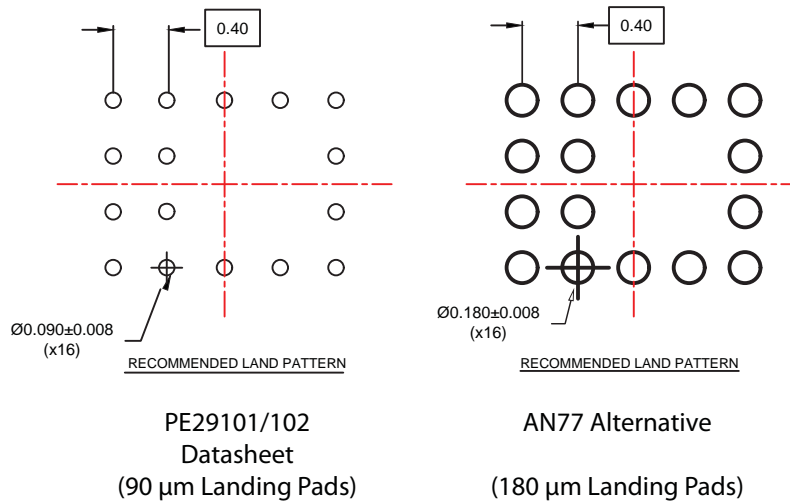
High-power transistors often require 2- or 3- $\mu\text{m}$  copper thickness to aid the heat dissipation and current conduction requirements of the applications circuit.

However, with the increased copper thickness, the small footprint for the PE29101/102 becomes difficult to manufacture.

The pSemi evaluation kit (EVK) actually uses a 180  $\mu\text{m}$  diameter pad for the PE29102. This is possible because the device pad spacing is 400  $\mu\text{m}$ . This spacing allows the pad size to be increased without any danger of pad or solder overlaps occurring during assembly and eases the board manufacture when using increased copper thicknesses for higher power circuits. The 180  $\mu\text{m}$  pad size also allows some misalignment in the placement of the device. This eases the assembly process and also allows the device to be hand-placed if circuit rework is necessary, easing prototype evaluation.

Figure 1 shows a comparison of land patterns for the PE29101/102 using 90 μm and 180 μm diameter pads.

Figure 1 ■ Land Pattern Comparison



## Conclusion

The footprint of the PE29101/2 stated in the data sheet causes concern with some board manufacturers. This application note shows that the pads' sizes can be increased without risk of misalignment or solder links between the device pads. This also enables the use of a thicker copper conductive layer for better thermal conduction by the surrounding circuits and the ability to conduct board re-work, if necessary.

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