Product Description

The PE9140 is an ultra-high linearity, passive broadband Quad MOSFET array with high dynamic range performance. This quad array operates with differential signals at all ports (RF, LO, IF), allowing mixers to be built that use LO powers from -7dBm to +20 dBm. Typical applications range from frequency up/down-conversion, IQ modulation and phase detection.

The PE9140 is optimized for space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than $10^9$ errors per bit/day. Fabricated in Peregrine’s patented UTSi® (Ultra Thin Silicon) CMOS technology, the PE9140 offers excellent RF performance and intrinsic radiation tolerance.

Figure 1. Functional Schematic Diagram

![Functional Schematic Diagram](image)

Table 1. DC Electrical Specifications @ +25 °C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain-Source Voltage</td>
<td>260</td>
<td>320</td>
<td>380</td>
<td>mV</td>
<td>$V_{GS} = +3V, I_{DS} = 40 mA$</td>
</tr>
<tr>
<td>$V_{DS}$ Match</td>
<td>Drain-Source Voltage Match</td>
<td>20</td>
<td>40</td>
<td></td>
<td>mV</td>
<td>$V_{DS_{max}} - V_{DS_{min}}$</td>
</tr>
<tr>
<td>$V_{T}$</td>
<td>Threshold Voltage</td>
<td>-100</td>
<td>40</td>
<td></td>
<td>mV</td>
<td>$V_{DS} = 0.1V; per ASTM F617-00$</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>Drain-Source ‘ON’ Resistance</td>
<td>6.5</td>
<td>7.75</td>
<td>9.5</td>
<td>Ω</td>
<td>$V_{GS} = +3V, I_{DS} = 40 mA$</td>
</tr>
</tbody>
</table>

Table 2. Mechanical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>586x716</td>
<td></td>
<td></td>
<td>µm</td>
<td></td>
</tr>
<tr>
<td>Wafer thickness</td>
<td>7.5</td>
<td>8.0</td>
<td>8.5</td>
<td>mils</td>
<td></td>
</tr>
<tr>
<td>Wafer Size</td>
<td>150</td>
<td></td>
<td></td>
<td>mm</td>
<td></td>
</tr>
</tbody>
</table>
Electrostatic Discharge (ESD) Precautions

This MOSFET device has minimally protected inputs and is highly susceptible to ESD damage. When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Device Description

The PE9140 passive broadband Quad MOSFET array is designed for use in up-conversion and down-conversion applications for high performance systems.

The PE9140 is an ideal mixer core for a wide range of mixer products, including module level solutions that incorporate baluns or other single-ended matching structures enabling three-port operation.

The performance level of this passive mixer is made possible by the very high linearity afforded by Peregrine’s UTSi CMOS process.

Table 2. Pin Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IF1</td>
<td>IF Output Connection (Drain)</td>
</tr>
<tr>
<td>2</td>
<td>RF1</td>
<td>RF Input Connection (Source)</td>
</tr>
<tr>
<td>3</td>
<td>RF2</td>
<td>RF Input Connection (Source)</td>
</tr>
<tr>
<td>4</td>
<td>LO2</td>
<td>LO Input Connection (Gate)</td>
</tr>
<tr>
<td>5</td>
<td>LO1</td>
<td>LO Input Connection (Gate)</td>
</tr>
<tr>
<td>6</td>
<td>IF2</td>
<td>IF Output Connection (Drain)</td>
</tr>
</tbody>
</table>

Table 3. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter/Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TST</td>
<td>Storage temperature range</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TOP</td>
<td>Operating temperature range</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>VDC + AC</td>
<td>Maximum DC plus peak AC voltage across Drain-Source</td>
<td>±3.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VDC + AC</td>
<td>Maximum DC plus peak AC voltage across Gate-Drain or Gate-Source</td>
<td>±4.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VESD</td>
<td>ESD Sensitive Device</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
Figure 3. Typical Schematic for a 1700 MHz to 2200 MHz Application

![Schematic Diagram]

Note: L1 and L2 provide LO port matching for optimum performance. Typical gate capacitance is approximately 2.5 pF.

Table 4. Typical Performance in a 1700 MHz to 2200 MHz Application @ +25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range**</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO</td>
<td>1630</td>
<td>--</td>
<td>2130</td>
<td>MHz</td>
</tr>
<tr>
<td>RF</td>
<td>1700</td>
<td>--</td>
<td>2200</td>
<td>MHz</td>
</tr>
<tr>
<td>IF</td>
<td>70</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Conversion Loss**</td>
<td>6.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(Includes balun losses)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation**</td>
<td>30</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>LO-RF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO-IF</td>
<td>26</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input IP3**</td>
<td>33</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Input 1 dB Compression**</td>
<td>23</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

** Data taken on an Evaluation Board narrow-band tuned to cover the 1700 MHZ TO 2200 MHZ band, IF = 70MHz low-side, LO drive = 17dBm.
Typical Performance Plots in a 1700 MHZ TO 2200 MHZ Application @ +25 °C

Figure 4. IIP3 & Conversion Loss vs. LO Power

Figure 5. IIP3 & Conversion Loss vs. Frequency

Figure 6. LO-RF & LO-IF Isolation
Figure 7. Typical Schematic for a 54 MHz to 864 MHz Application

Note: L1 and L2 provide LO port matching for optimum performance. Typical gate capacitance is approximately 2.5 pF.

Table 5. Typical Performance in a 54 MHz to 864 MHz Application @ +25 °C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range**</td>
<td>1116</td>
<td>--</td>
<td>1926</td>
<td>MHz</td>
</tr>
<tr>
<td>LO</td>
<td>54</td>
<td>--</td>
<td>864</td>
<td>MHz</td>
</tr>
<tr>
<td>IF</td>
<td>1062</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Conversion Loss**</td>
<td></td>
<td>6.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(Includes balun losses)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation**</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>LO-RF</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>LO-IF</td>
<td>28</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input IP3**</td>
<td>23</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Input 1 dB Compression**</td>
<td>13</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

** Data taken on an Evaluation Board tuned for a broadband 54 MHz to 864 MHz application, IF = 1062 MHz, RF drive = -5 dBm, LO drive = 10 dBm.
Typical Performance Plots in a 54 MHz to 864 MHz Application @ +25 °C

Figure 8. IIP3 vs. Frequency

Figure 9. Conversion Loss vs. Frequency

Figure 10. LO-RF & LO-IF Isolation
Figure 11. Dice and Wafer Processing Flow

1. Wafer Processing
   - Visual Inspection
2. PCM and WLR Test
3. Aracor X-ray Test
4. Thin and Dice
   - Visual Inspection
     - Mil std 883 Method 2010

Flow:
- Cond A
- Cond B

Pick and Plate
- Die in waﬄe pack 2010 Cond B

Ship EQM Die

Assemble Die in Ceramic Package
- Per spec 01/0032

Tri -temp Pre BI Test
- per product Test specification

Is Yield Acceptable?
- No ⇒ Reject Lot

Post BI Tri-Temp Test
- PDA < 5%
  - Yes ⇒ Complete Element Evaluation
    - Testing per 01/0032
  - No ⇒ Reject Lot

Does Lot Pass Element Evaluation?
- No ⇒ Reject Lot

Ship Flight Die

Cond A Die

Per spec 01/0032

Tri -temp Pre BI Test
- per product Test specification

Is Yield Acceptable?
- No ⇒ Reject Lot

Post BI Tri-Temp Test
- PDA < 5%
  - Yes ⇒ Complete Element Evaluation
    - Testing per 01/0032
  - No ⇒ Reject Lot

Does Lot Pass Element Evaluation?
- No ⇒ Reject Lot
Die Packaging

Peregrine will ship in Standard Die Carrier Package (waffle pack) shown in Figure 12.

Standard Die Carrier Package

- Chips which have been electrically probed, inked, visually inspected, and diced, will be packaged in 2”x2” standard die carrier packages (i.e. Waffle Packs)
- Standard die carrier packages protect the product from mechanical damage during shipment and prevent individual die from contacting one another
- Standard die carrier packages are sealed in static and moisture protective bags to protect the product from static discharge, moisture and other contamination by sealing in the proper static and moisture protective bags.
- Die are held in cavities with a defined matrix. Ideal for small volumes.
- Die orientation is indicated on the label.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection – dice in carriers, geometry side up.
- Standard die carrier package holds 100 dice.

Figure 12. Waffle Pack

Die Qualification Flow

Figure 11 shows the generic qualification flow for the PE9140 die. Reference Peregrine Document 01/0032 (Peregrine Element Evaluation).

Wafer and Die Package, Storage and Preservation

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

- Product should be stored in original unopened packaging or, once opened, in a Nitrogen purged cabinet at room temperature (45% +/- 15% RH controlled environment).
- Sawn wafers mounted on dicing tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used for mounting the product. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- In all cases, the customer must determine the applicability of extended storage durations and conditions with respect to their assembly process and end product criteria.

Die Handling

All die products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263. ESD wrist strap and cord must be worn at a static safe workstation to eliminate failures due to ESD. Product must be handled only in a class 10,000 or better designated clean room environment.

Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used. Automated Wafer and Die
Handling systems are readily available and provide the highest degree of protection and consistency to the handling operation.

**Recommended Dice Assembly Procedure**

**Cleaning**

Dice supplied in die or wafer form do not require cleaning prior to assembly.

**Die Attach**

The Peregrine Semiconductor die substrate is sapphire and the recommended die attach operation uses epoxy die attach adhesive. The eutectic die attach method does not work with sapphire substrates.

**Bonding**

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about three times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. Aluminum 1-mil wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated. Note the bonding pad material is aluminum.

**Shipping Method**

Standard die carrier packages and wafer packages are vacuum-sealed with desiccant inside an ESD shielding moisture barrier bag. Sealed product is then placed inside corrugated cardboard box surrounded by bubble wrap or foam for maximum protection during shipment.

**Table 6. Ordering Information**

<table>
<thead>
<tr>
<th>Order Code</th>
<th>Part Marking</th>
<th>Description</th>
<th>Package</th>
<th>Shipping Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>PE9140-99</td>
<td>FD91400</td>
<td>PE9140-DIE-100W</td>
<td>Waffle Pack</td>
<td>100 units/Waffle Pack</td>
</tr>
</tbody>
</table>
Sales Offices

United States
Peregrine Semiconductor Corp.
6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

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Peregrine Semiconductor Europe
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Tel 33-1-47-41-91-73
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1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

For a list of representatives in your area, please refer to our Web site at: http://www.peregrine-semi.com

Data Sheet Identification

Advance Information
The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification
The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification
The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a PCN (Product Change Notice).

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