

# PE43713

Document Category: Product Specification

UltraCMOS® RF Digital Step Attenuator, 9 kHz–6 GHz



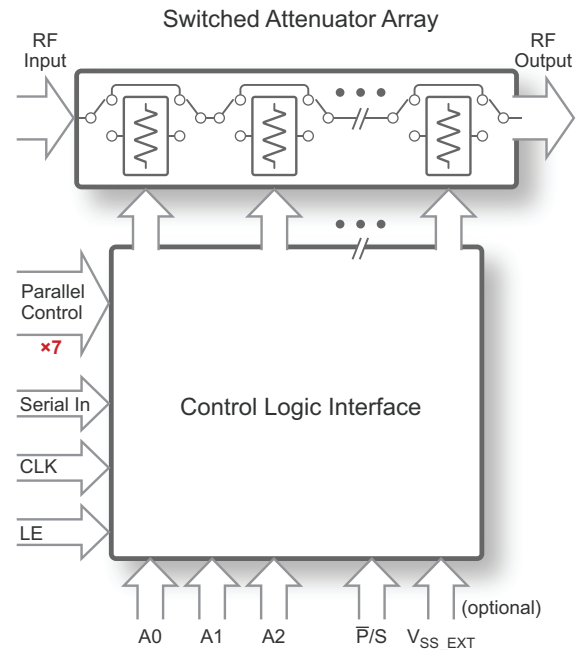
## Features

- Flexible attenuation steps of 0.25 dB, 0.5 dB and 1 dB up to 31.75 dB
- Glitchless attenuation state transitions
- Monotonicity: 0.25 dB up to 4 GHz, 0.5 dB up to 5 GHz, and 1 dB up to 6 GHz
- Extended +105 °C operating temperature
- Parallel and serial programming interfaces with serial addressability
- Packaging: 32-lead 5 × 5 mm QFN

## Applications

- Test and measurement (T&M)
- General-purpose RF attenuator

Figure 1 • PE43713 functional diagram



## Product description

The PE43713 is a 50Ω, HaRP™ technology-enhanced, 7-bit RF digital step attenuator (DSA) that supports a broad frequency range from 9 kHz to 6 GHz. It features glitchless attenuation state transitions, supports 1.8V control voltage, and includes an extended operating temperature range to +105 °C with an optional  $V_{SS\_EXT}$  bypass mode to improve spurious performance, making this device ideal for test and measurement.

The PE43713 is a pin-compatible and upgraded version of the pSemi PE43703. An integrated digital control interface supports both serial addressable and parallel programming of the attenuation, including the ability to program an initial attenuation state at power-up.

The PE43713 covers a 31.75 dB attenuation range in 0.25-dB, 0.5-dB, and 1-dB steps. It maintains 0.25-dB monotonicity through 4 GHz, 0.50-dB monotonicity through 5 GHz, and 1-dB monotonicity through 6 GHz. No external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43713 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

## Absolute maximum ratings

Exceeding the absolute maximum ratings listed in **Table 1** can cause permanent damage. Restrict operations to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

### ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

### Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

*Table 1 • PE43713 absolute maximum ratings*

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	$V_{DD}$	-0.3	5.5	V
Digital input voltage	-	-0.3	3.6	V
RF input power, 50Ω: 9 kHz–48 MHz >48 MHz–6 GHz	-	-	<b>Figure 5 +31</b>	dBm
Storage temperature range	-	-65	+150	°C
ESD voltage HBM, all pins <sup>(1)</sup>	-	-	3000	V
ESD voltage CDM, all pins <sup>(2)</sup>	-	-	1000	V
<b>Notes:</b>				
1) Human body model (MIL-STD 883 Method 3015).				
2) Charged device model (JEDEC JESD22-C101).				

## Recommended operating conditions

**Table 2** lists the PE43713 recommending operating conditions. Do not operate devices outside the recommended operating conditions listed below.

*Table 2 • PE43713 recommended operating conditions*

Parameter	Symbol	Min	Typ	Max	Unit
<b>Normal mode, <math>V_{SS\_EXT} = 0V^{(1)}</math></b>					
Supply voltage	$V_{DD}$	2.3	–	5.5	V
Supply current	$I_{DD}$	–	150	200	$\mu A$
<b>Bypass mode, <math>V_{SS\_EXT} = -3.4V^{(2)}</math></b>					
Supply voltage ( $V_{DD} \geq 3.4V$ , see <b>Table 3</b> for the full specification compliance)	$V_{DD}$	2.7	3.4	5.5	V
Supply current	$I_{DD}$	–	50	80	$\mu A$
Negative supply voltage	$V_{SS\_EXT}$	–3.6	–	–2.4	V
Negative supply current	$I_{SS}$	–40	–16	–	$\mu A$
<b>Normal or bypass mode</b>					
Digital input high	–	1.17	–	3.6	V
Digital input low	–	–0.3	–	0.6	V
Digital input current	–	–	–	17.5	$\mu A$
RF input power, CW: <sup>(3)</sup> 9 kHz–48 MHz >48 MHz–6 GHz	–	–	–	<b>Figure 5</b> +23	dBm
RF input power, pulsed: <sup>(4)</sup> 9 kHz–48 MHz >48 MHz–6 GHz	–	–	–	<b>Figure 5</b> +28	dBm
Operating temperature range	$T_{OP}$	–40	+25	+105	$^{\circ}C$
<b>Notes:</b>					
1) Normal mode: Connect $V_{SS\_EXT}$ (pin 20) to GND ( $V_{SS\_EXT} = 0V$ ) to enable the internal negative voltage generator.					
2) Bypass mode: Use $V_{SS\_EXT}$ (pin 20) to bypass and disable the internal negative voltage generator.					
3) 100% duty cycle, all bands, 50 $\Omega$ .					
4) Pulsed, 5% duty cycle of 4620- $\mu s$ period, 50 $\Omega$ .					

## Electrical specifications

**Table 3** lists the PE43713 key electrical specifications at 25 °C,  $RF1 = RF_{IN}$ ,  $RF2 = RF_{OUT}$  ( $Z_S = Z_L = 50\Omega$ ), unless otherwise specified.

- Normal mode:  $V_{DD} = 3.3V$  and  $V_{SS\_EXT} = 0V$ . To enable the internal negative voltage generator, connect  $V_{SS\_EXT}$  (pin 20) to GND ( $V_{SS\_EXT} = 0V$ ).
- Bypass mode:  $V_{DD} = 3.4V$  and  $V_{SS\_EXT} = -3.4V$ . To bypass and disable the internal negative voltage generator, use  $V_{SS\_EXT}$  (pin 20).

**Table 3 • PE43713 electrical specifications**

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency	–	–	9 kHz	–	6 GHz	As shown
Attenuation range	0.25 dB step 0.5 dB step 1 dB step	–	–	0–31.75 0–31.50 0–31.00	–	dB
Insertion loss	–	9 kHz–1.0 GHz 1.0–2.2 GHz 2.2–4.0 GHz 4.0–6.0 GHz	–	1.3 1.6 1.95 2.45	1.5 1.85 2.4 2.8	dB
Attenuation error	<b>0.25-dB step</b>					
	0–8 dB	9 kHz–2.2 GHz	–	–	$\pm(0.20 + 1.5\%$ of attenuation setting)	dB
	8.25–31.75 dB	9 kHz–2.2 GHz	–	–	$\pm(0.20 + 2.0\%$ of attenuation setting)	dB
	0–31.75 dB	>2.2–3.0 GHz	–	–	$\pm(0.15 + 3.0\%$ of attenuation setting)	dB
	0–31.75 dB	>3.0–4.0 GHz	–	–	$\pm(0.25 + 3.5\%$ of attenuation setting)	dB
	<b>0.5-dB step</b>					
	0–8 dB	9 kHz–2.2 GHz	–	–	$\pm(0.20 + 1.5\%$ of attenuation setting)	dB
	8.5–31.5 dB	9 kHz–2.2 GHz	–	–	$\pm(0.20 + 2.0\%$ of attenuation setting)	dB
	0–31.5 dB	>2.2–3.0 GHz	–	–	$\pm(0.15 + 3.0\%$ of attenuation setting)	dB
	0–31.5 dB	>3.0–5.0 GHz	–	–	$\pm(0.25 + 5.0\%$ of attenuation setting)	dB

Table 3 • PE43713 electrical specifications (Cont.)

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Attenuation error	<b>1-dB step</b>					
	0–8 dB	9 kHz–2.2 GHz	–	–	±(0.20 + 1.5% of attenuation setting)	dB
	9–31 dB	9 kHz–2.2 GHz	–	–	±(0.20 + 2.0% of attenuation setting)	dB
	0–31 dB	>2.2–3.0 GHz	–	–	±(0.15 + 3.0% of attenuation setting)	dB
	0–31 dB	>3.0–5.0 GHz	–	–	±(0.25 + 5.0% of attenuation setting)	dB
	0–31 dB	>5.0–6.0 GHz	–	–	±(0.25 + 5.0% of attenuation setting)	dB
Return loss	Input port	9 kHz–6 GHz	–	18	–	dB
	Output port	9 kHz–4 GHz 4–6 GHz	–	13 15	–	dB
Relative phase	All states	9 kHz–4 GHz 4–6 GHz	–	27 42	–	deg
Input 0.1 dB compression point <sup>(1)</sup>	–	48 MHz–6 GHz	–	31	–	dBm
Input IP3	Two tones at +18 dBm with 20-MHz spacing	4 GHz 6 GHz	–	57 56	–	dBm
RF T <sub>rise</sub> /T <sub>fall</sub>	10%/90% RF	–	–	200	–	ns
Settling time <sup>(2)</sup>	RF settled to within 0.05 dB of the final value	–	–	1.6	–	µs
Switching time	50% CTRL to 90% or 10% RF	–	–	275	–	ns
Attenuation transient (envelope)	–	2 GHz	–	0.3	–	dB

**Notes:**

- 1) The input 0.1 dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
- 2) The PE43713 has a maximum 25 kHz switching rate in normal mode (pin 20 tied to ground). A faster switching rate is available in bypass mode (pin 20 tied to V<sub>SS\_EXT</sub>). The rate at which the PE43713 can be switched is then limited to the switching time as specified above. The switching frequency is defined as the speed at which the DSA can be toggled across the attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

## Optional external $V_{SS}$ control

For proper operation, the  $V_{SS\_EXT}$  control pin must be grounded or tied to the  $V_{SS}$  voltage specified in **Table 2**. When the  $V_{SS\_EXT}$  control pin is grounded, the FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spurious performance, apply  $V_{SS\_EXT}$  externally to bypass the internal negative voltage generator.

## Spurious-free performance

The typical spurious performance of the PE43713 in normal mode is  $-130$  dBm with  $V_{SS\_EXT}$  (pin 20) tied to ground. For spurious-free performance, disable the internal negative voltage generator by applying a negative voltage to  $V_{SS\_EXT}$  (pin 20).

## Glitchless attenuation state transitions

The PE43713 features a novel architecture to provide the best-in-class glitchless transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced ( $\leq 0.3$  dB) during attenuation state changes when compared to previous-generation DSAs.

## Truth tables

**Table 4–Table 6** list the PE43713 truth tables.

*Table 4 • Parallel truth table*

Parallel control setting							Attenuation setting RF1–RF2
D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

Table 5 • Serial address word truth table

Address word								Address setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

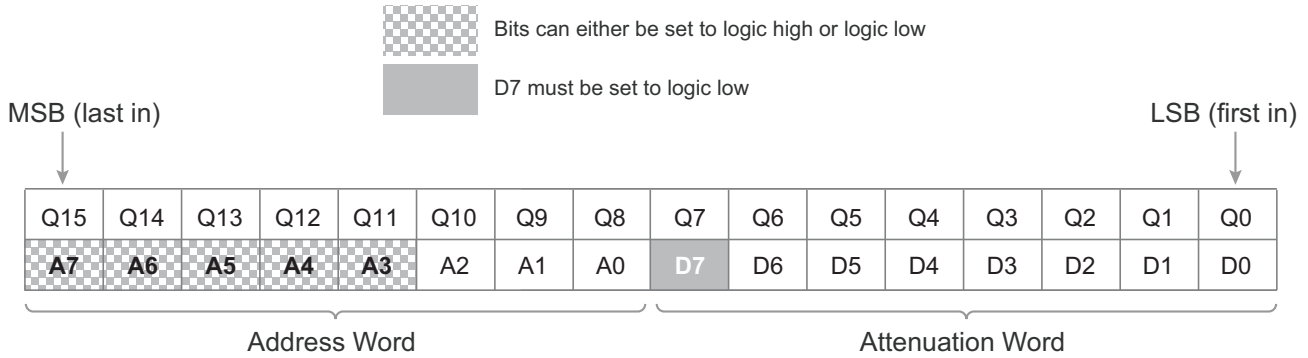
Table 6 • Serial attenuation word truth table

Attenuation word								Attenuation setting RF1–RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

## Serial-addressable register map

Figure 2 shows the PE43713 serial-addressable register map.

Figure 2 • Serial-addressable register map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 18.25 dB state at address 3:

$$4 \times 18.25 = 73$$

$$73 \rightarrow 01001001$$

Address Word: XXXXX011  
Attenuation Word: 01001001  
Serial Input: XXXXX01101001001

## Programming options

### Parallel or serial selection

You can use either a parallel or serial-addressable interface to control the PE43713. The  $\overline{P/S}$  bit provides this selection:

- $\overline{P/S}$  = LOW selects the parallel interface.
- $\overline{P/S}$  = HIGH selects the serial interface.

### Parallel mode interface

The parallel interface consists of seven CMOS-compatible control lines that select the preferred attenuation state, as shown in **Table 4**.

The parallel interface timing requirements are defined by the parallel interface timing diagram (**Figure 4**), the parallel and direct AC characteristics (**Table 9**), and the switching time (**Table 3**).

For latched parallel programming, hold the Latch Enable (LE) LOW while changing the attenuation state control values. To latch the new attenuation state into the device, pulse LE HIGH-to-LOW per **Figure 4**.

For direct parallel programming, pull the LE line HIGH. Changing the attenuation state control values changes the device state to the new attenuation. Direct mode is ideal for manual control of the device using hardware, switches, or jumpers.

In parallel mode, the Serial-In (SI) and Clock (CLK) pins are "don't care," and can be tied to logic LOW or logic HIGH.

### Serial-addressable interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words consisting of 8-bits each:

- The first is the attenuation word, which controls the DSA state.
- The second is the address word, which is compared to the static (or programmed) logical states of the A0, A1, and A2 digital inputs.

If an address matches, the DSA changes state; otherwise its current state remains unchanged. **Figure 3** shows an example timing diagram for programming a state. Ground all parallel control inputs when using the DSA in serial-addressable mode.

The serial-addressable interface is controlled using three CMOS-compatible signals: SI, CLK, and LE. The SI and CLK inputs allow data to be serially entered into the shift register. The serial data is clocked in LSB first.

To prevent the attenuator value from changing as data is entered, hold LE LOW while the shift register loads. To latch the new data into the DSA, toggle the LE input HIGH then bring it LOW again.

- **Table 5** lists the address word table.
- **Table 6** lists the attenuation word table.
- **Figure 2** shows a serial register programming example.
- **Figure 3** shows the serial-addressable timing diagram.

## Power-up control settings

The PE43713 always initializes to the maximum attenuation setting (31.75 dB) on power-up for both the serial addressable and latched parallel modes of operation and remains in this setting until you latch in the next programming word. In direct parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the parallel control pins before power-up. In this mode, there is a 400- $\mu$ s delay between the time that the DSA is powered-up to the time that the preferred state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to your defined state. If the control pins are left floating in this mode during power-up, the device defaults to the minimum attenuation setting (the insertion loss state).

Dynamic operation between the serial and parallel programming modes is possible:

- If the DSA powers up in serial mode ( $\overline{P/S} = \text{HIGH}$ ), all the parallel control inputs DI[6:0] must be set to logic LOW. Before toggling to parallel mode, the DSA must be programmed serially to ensure that D[7] is set to logic LOW.
- If the DSA powers up in either latched or direct parallel mode, all parallel pins DI[6:0] must be set to logic LOW before toggling to serial-addressable mode ( $\overline{P/S} = \text{HIGH}$ ), and held LOW until the DSA has been programmed serially to ensure that bit D[7] is set to logic LOW.

The sequencing is only required once upon power-up. When completed, you can toggle the DSA between the serial and parallel programming modes at will.

Figure 3 • Serial-addressable timing diagram

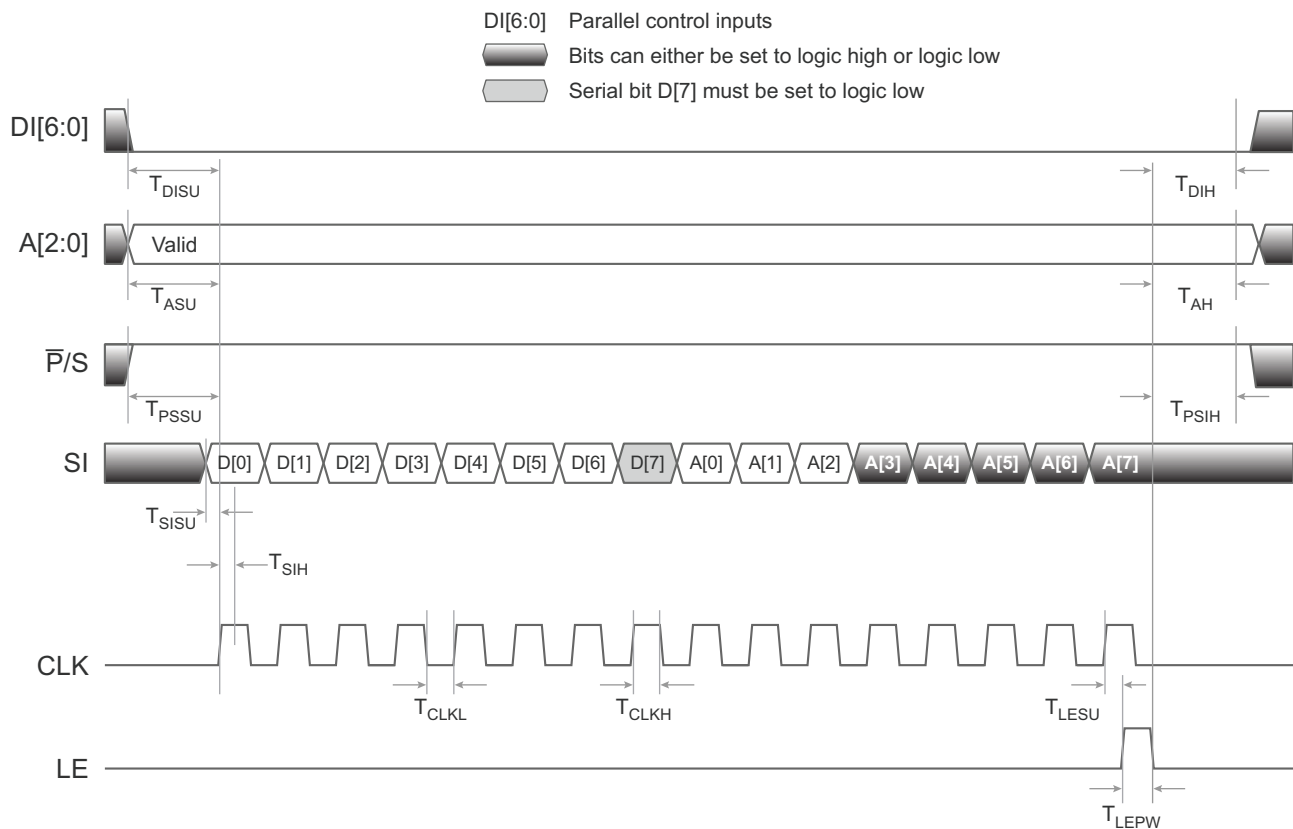


Figure 4 • Latched-parallel/direct-parallel timing diagram

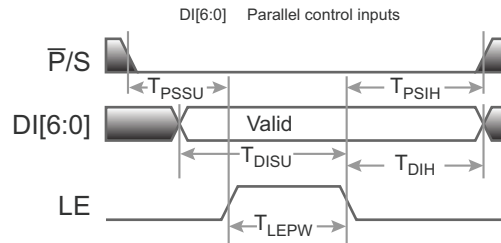


Table 7 • Latch and clock specifications

Latch Enable	Shift clock	Function
0	↑	Shift register clocked
↑	X	Contents of shift register transferred to attenuator core

Table 8 • Serial interface AC characteristics(\*)

Parameter or condition	Symbol	Min	Max	Unit
Serial clock frequency	$F_{CLK}$	–	10	MHz
Serial clock HIGH time	$T_{CLKH}$	30	–	ns
Serial clock LOW time	$T_{CLKL}$	30	–	ns
Last serial clock rising edge setup time to Latch Enable rising edge	$T_{LESU}$	10	–	ns
Latch Enable minimum pulse width	$T_{LEPW}$	30	–	ns
Serial data setup time	$T_{SISU}$	10	–	ns
Serial data hold time	$T_{SIH}$	10	–	ns
Parallel data setup time	$T_{DISU}$	100	–	ns
Parallel data hold time	$T_{DIH}$	100	–	ns
Address setup time	$T_{ASU}$	100	–	ns
Address hold time	$T_{AH}$	100	–	ns
Parallel/serial setup time	$T_{PSSU}$	100	–	ns
Parallel/serial hold time	$T_{PSIH}$	100	–	ns

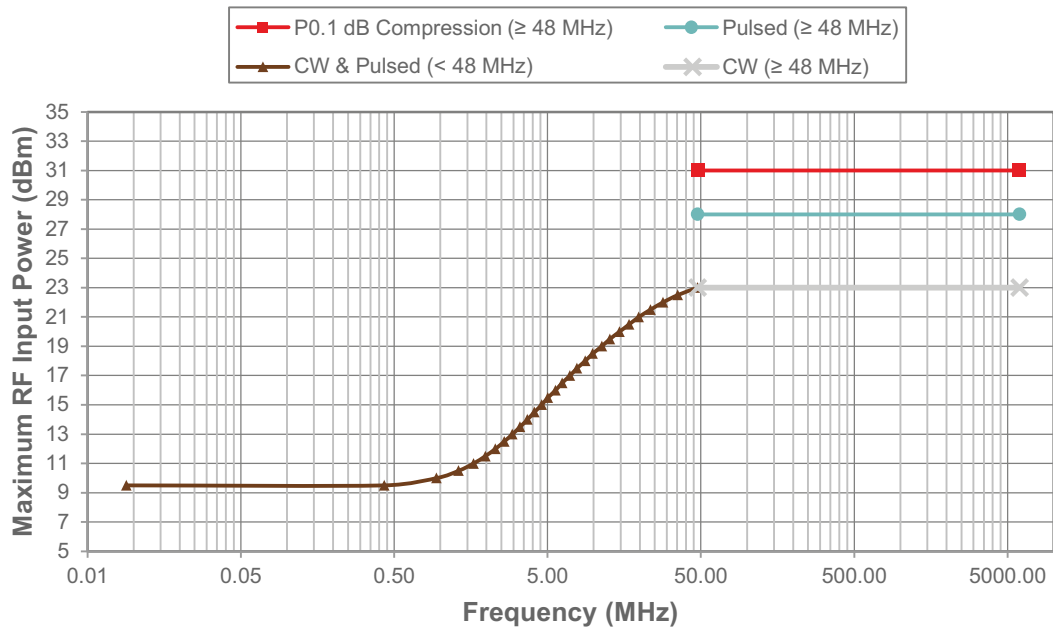
Note: \*  $V_{DD} = 3.3V$  or  $5.0V$ ,  $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 9 • Parallel and direct interface AC characteristics<sup>(\*)</sup>

Parameter or condition	Symbol	Min	Max	Unit
Latch Enable minimum pulse width	$T_{LEPW}$	30	–	ns
Parallel data setup time	$T_{DISU}$	100	–	ns
Parallel data hold time	$T_{DIH}$	100	–	ns
Parallel/serial setup time	$T_{PSSU}$	100	–	ns
Parallel/serial hold time	$T_{PSIH}$	100	–	ns
<b>Note:</b> * $V_{DD} = 3.3V$ or $5.0V$ , $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ , unless otherwise specified.				

## Power de-rating curve

Figure 5 • Power de-rating curve, 9 kHz–6 GHz, –40 to +105 °C ambient, 50Ω



## Typical performance data

Figure 6–Figure 32 show the typical performance data at 25 °C and  $V_{DD} = 3.3V$ ,  $RF1 = RF_{IN}$ ,  $RF2 = RF_{OUT}$  ( $Z_S = Z_L = 50\Omega$ ) unless otherwise specified.

Figure 6 • Insertion loss vs. temperature

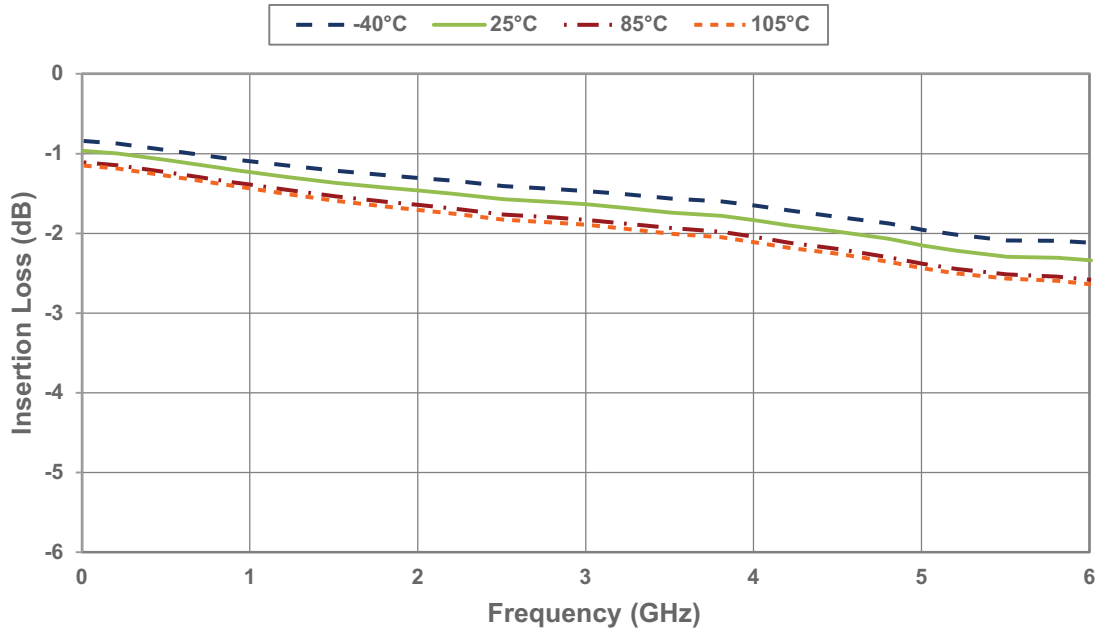


Figure 7 • Input return loss vs. attenuation setting

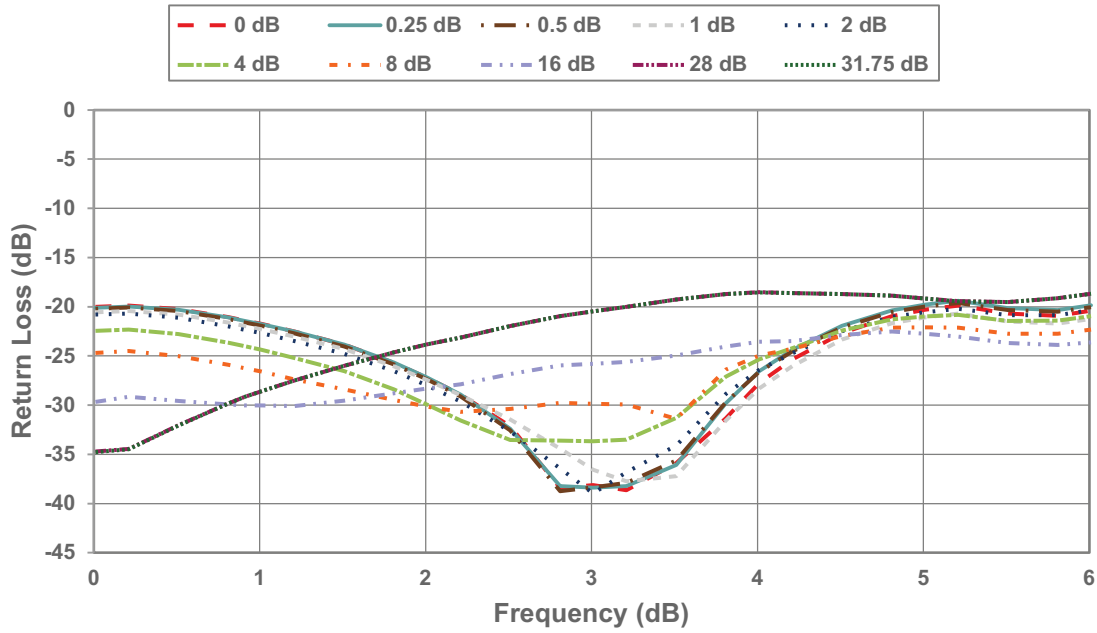


Figure 8 • Output return loss vs. attenuation setting

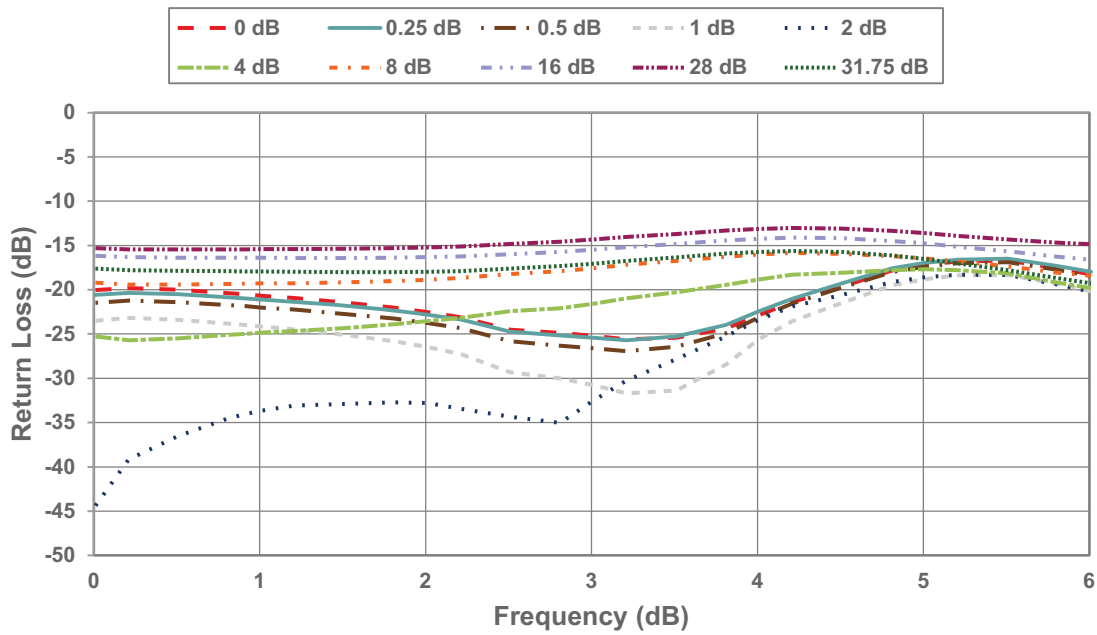


Figure 9 • Input return loss for 16 dB attenuation setting vs. temperature

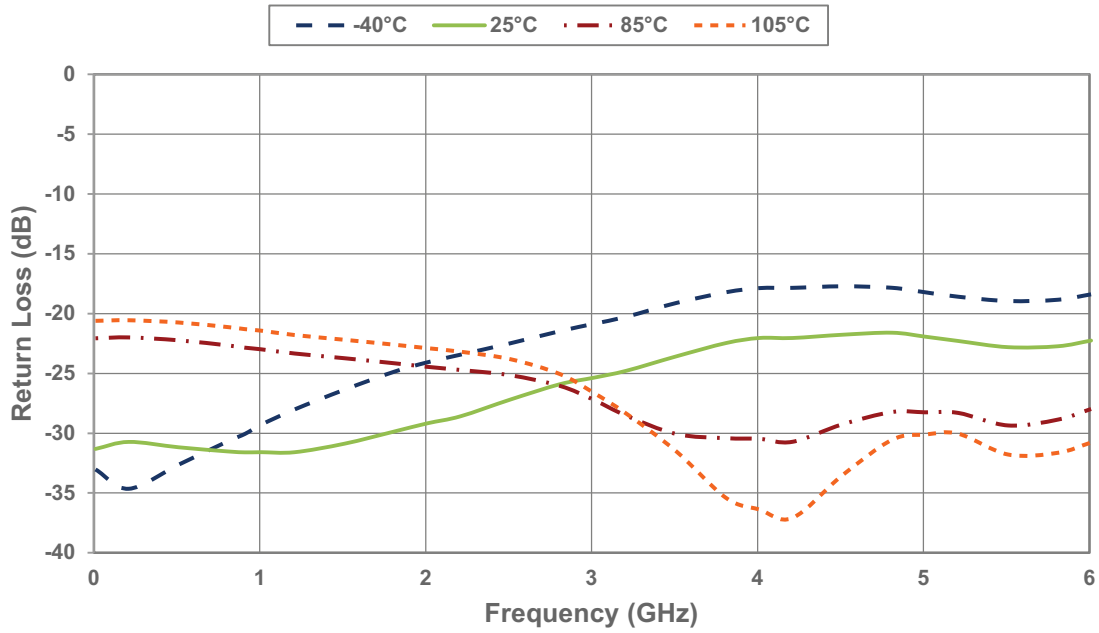


Figure 10 • Output return loss for 16 dB attenuation setting vs. temperature

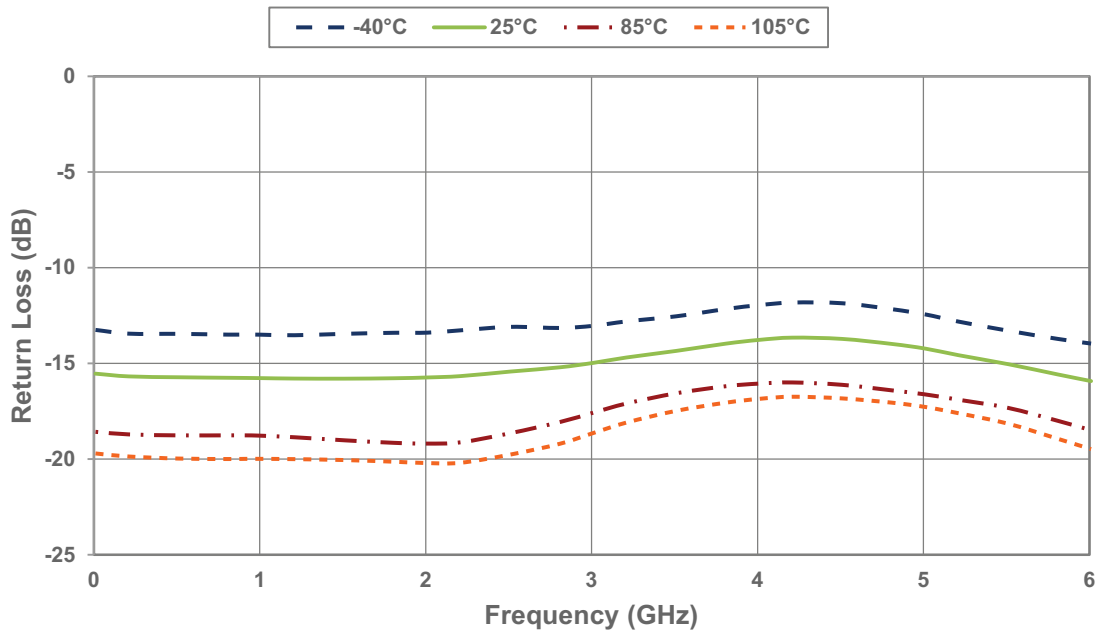


Figure 11 • Relative phase error vs. attenuation setting

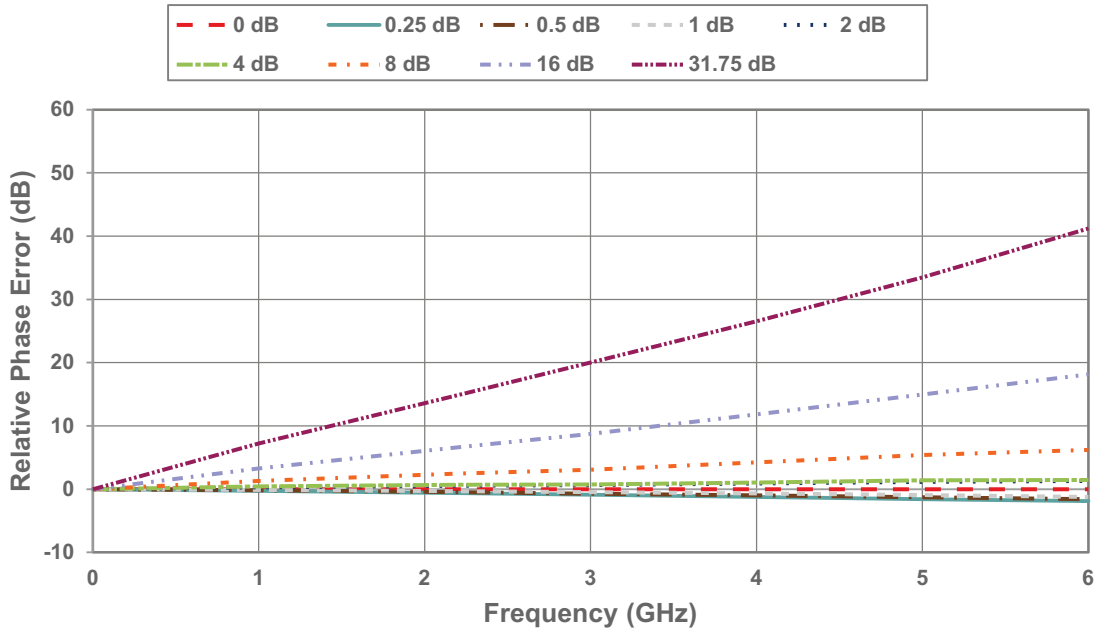


Figure 12 • Relative phase error for 31.75 dB attenuation setting vs. frequency

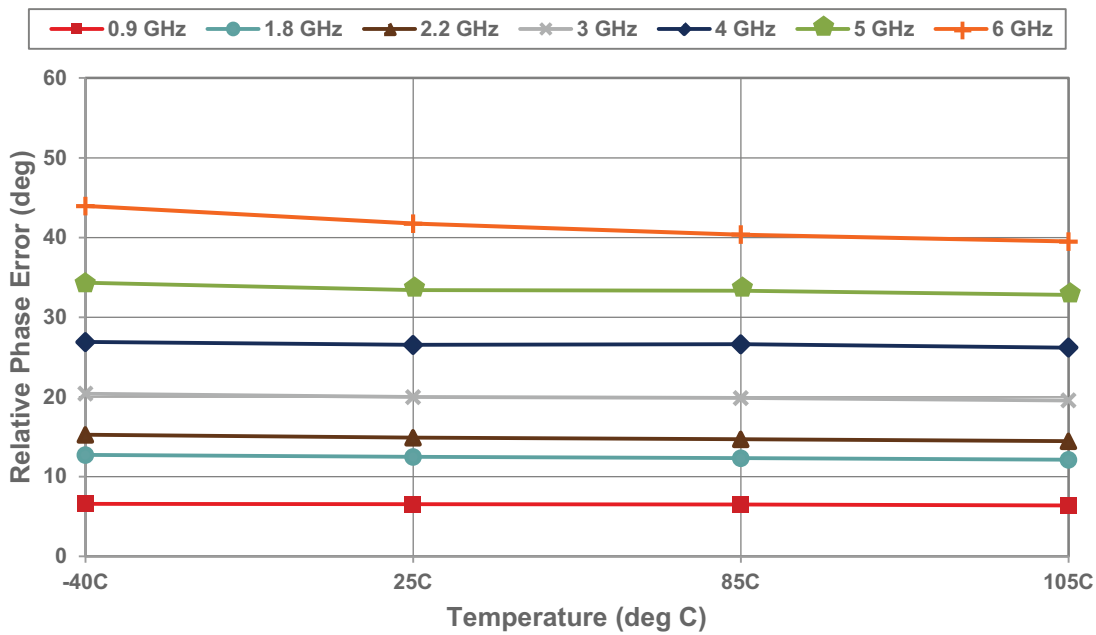


Figure 13 • Attenuation error @ 900 MHz vs. temperature

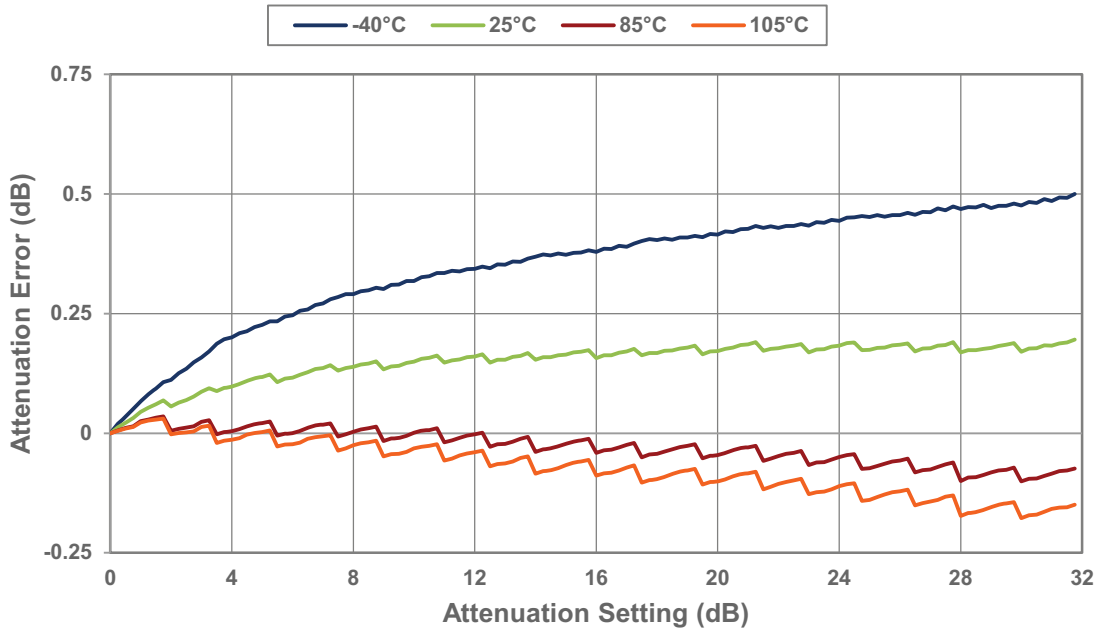


Figure 14 • Attenuation error @ 1800 MHz vs. temperature

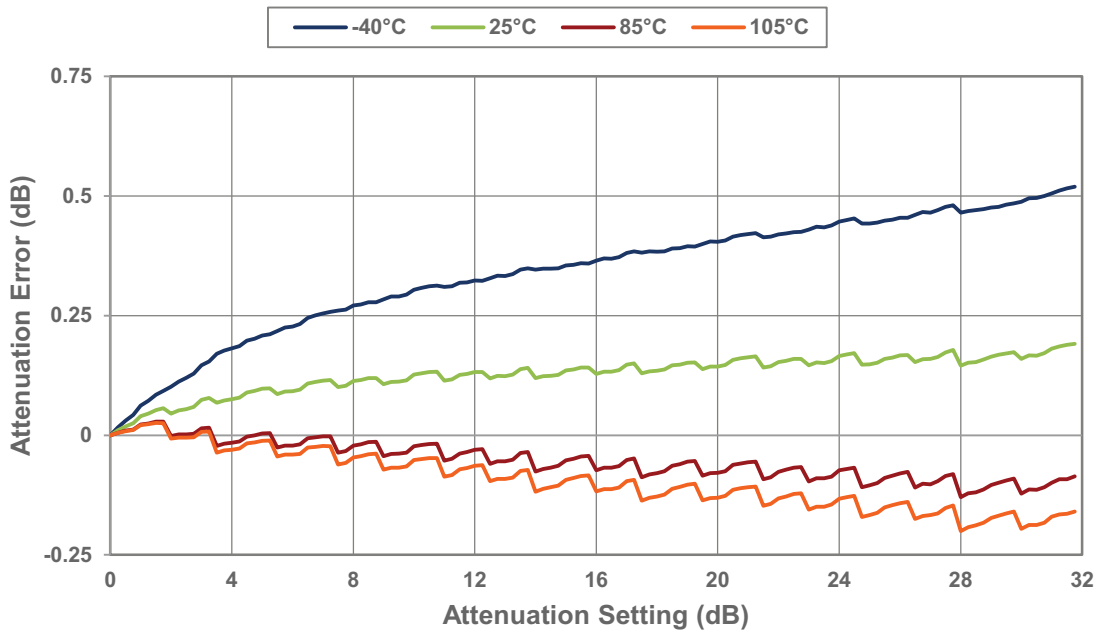


Figure 15 • Attenuation error @ 2200 MHz vs. temperature

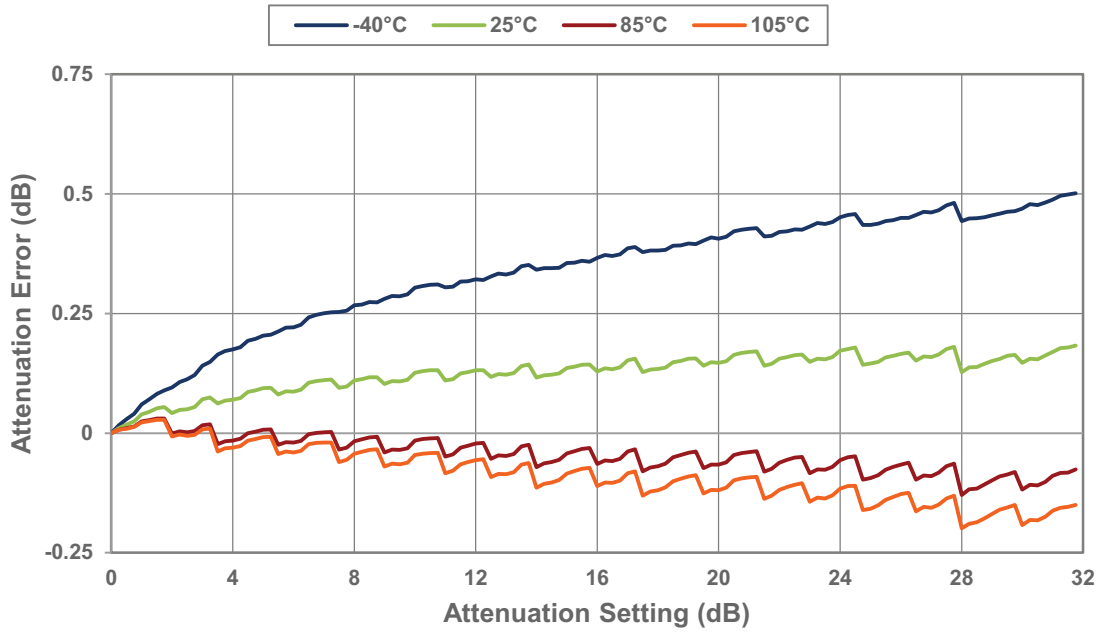


Figure 16 • Attenuation error @ 3000 MHz vs. temperature

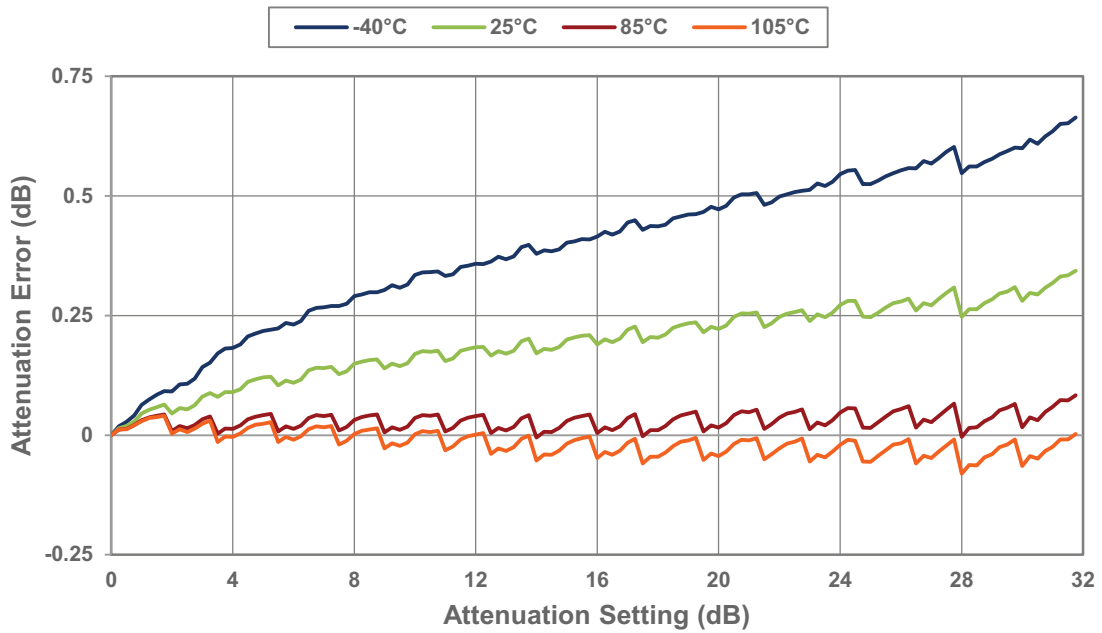


Figure 17 • Attenuation error @ 4000 MHz vs. temperature

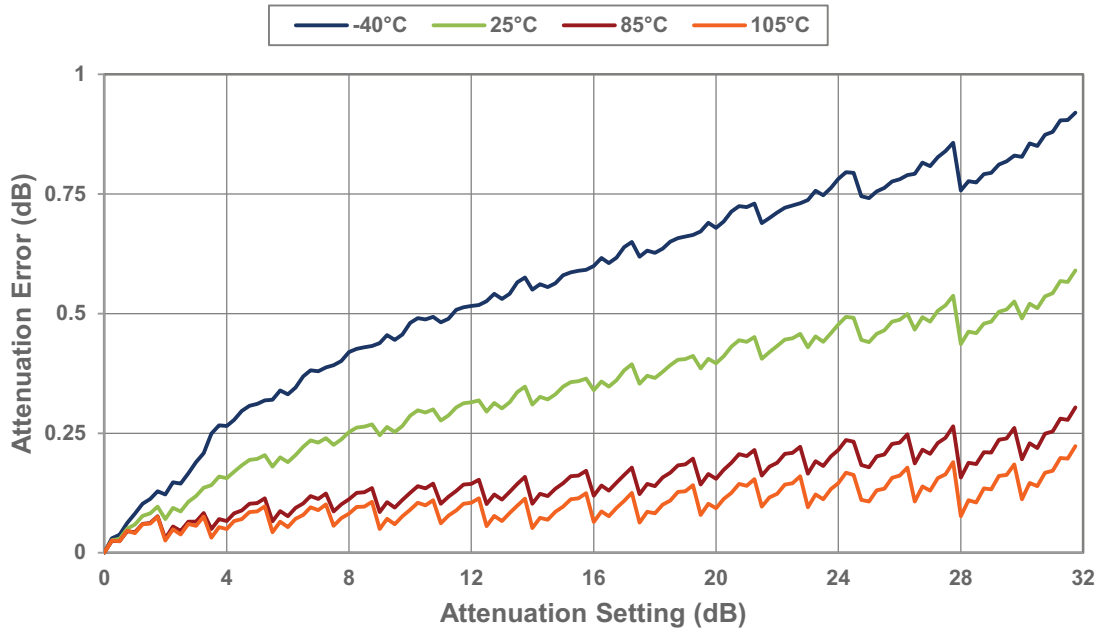


Figure 18 • IIP3 vs. attenuation setting

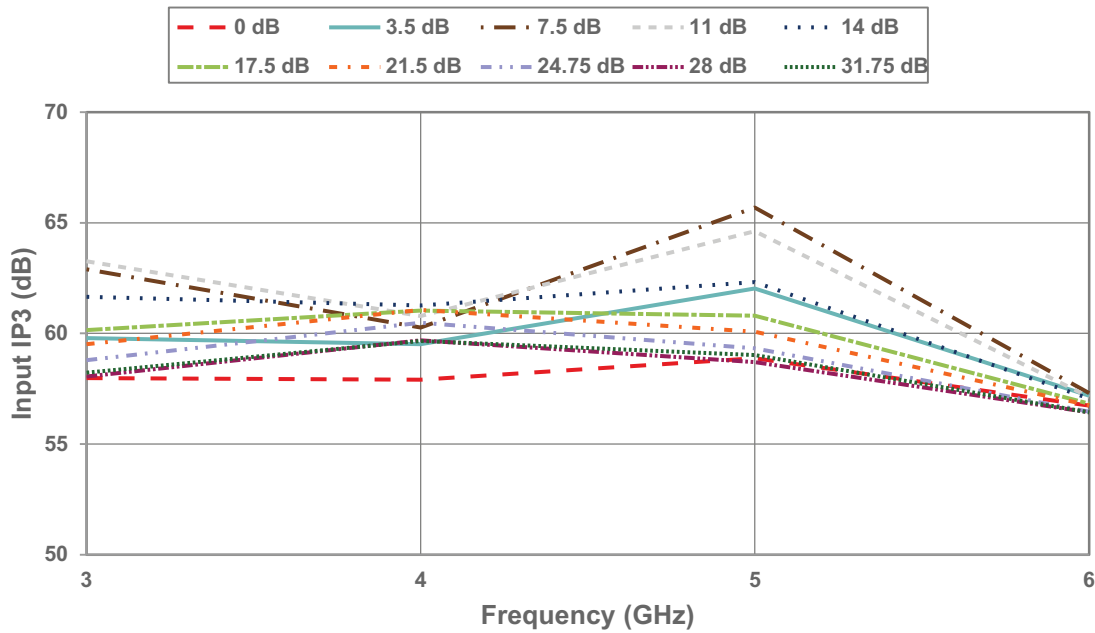
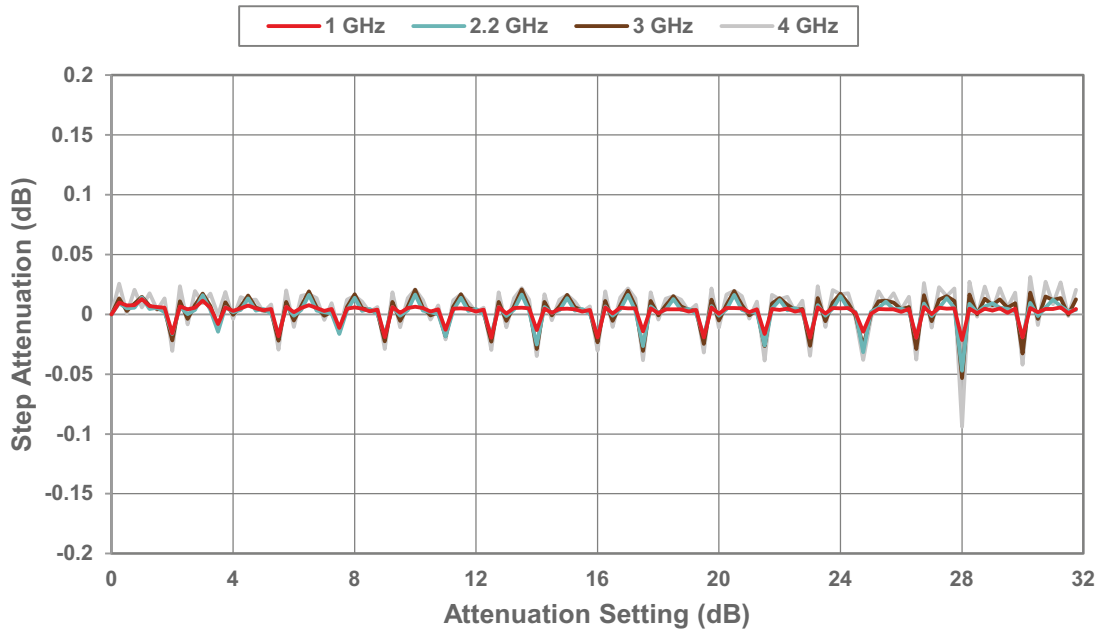


Figure 19 • 0.25-dB step attenuation vs. frequency<sup>(\*)</sup>



Note: \* Monotonicity is held so long as step attenuation does not cross below  $-0.25$  dB.

Figure 20 • 0.25-dB step, actual vs. frequency

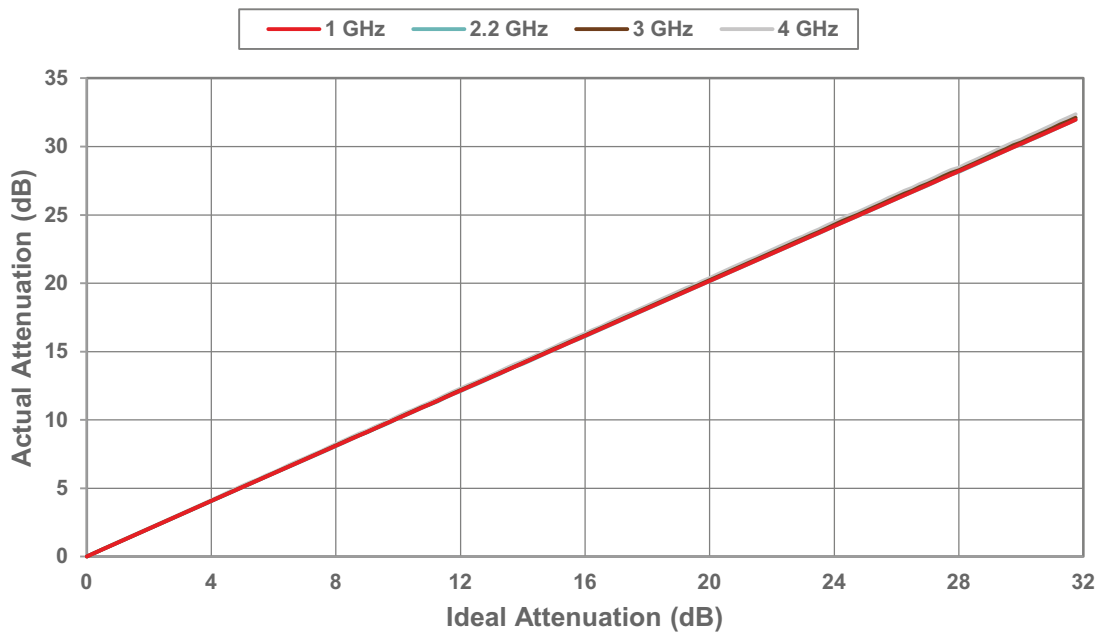


Figure 21 • 0.25 dB major state bit error vs. attenuation setting

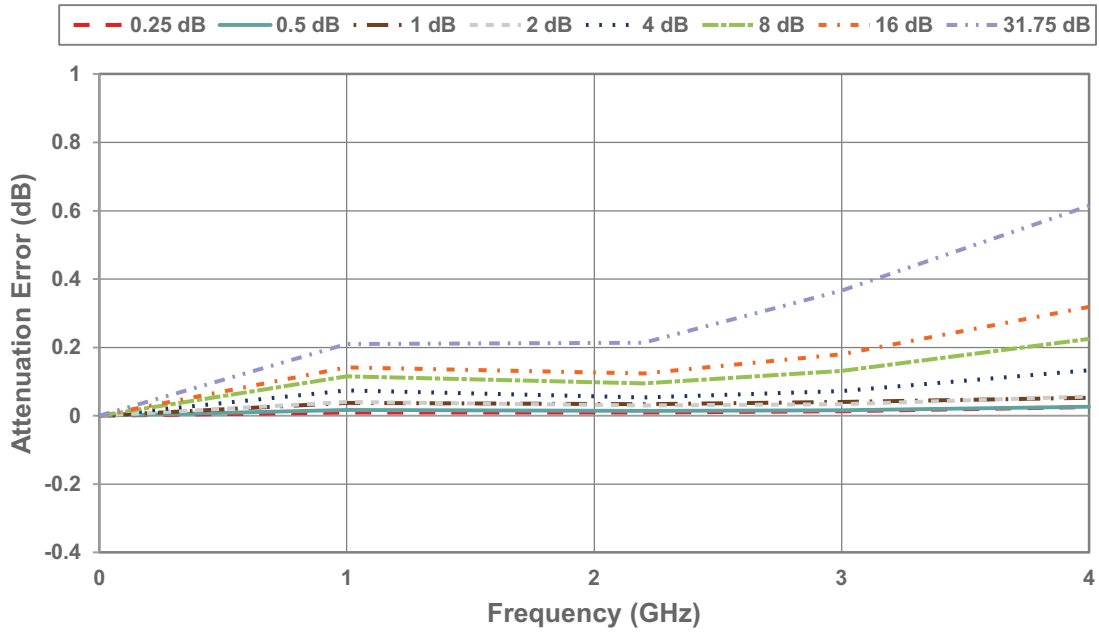


Figure 22 • 0.25 dB attenuation error vs. frequency

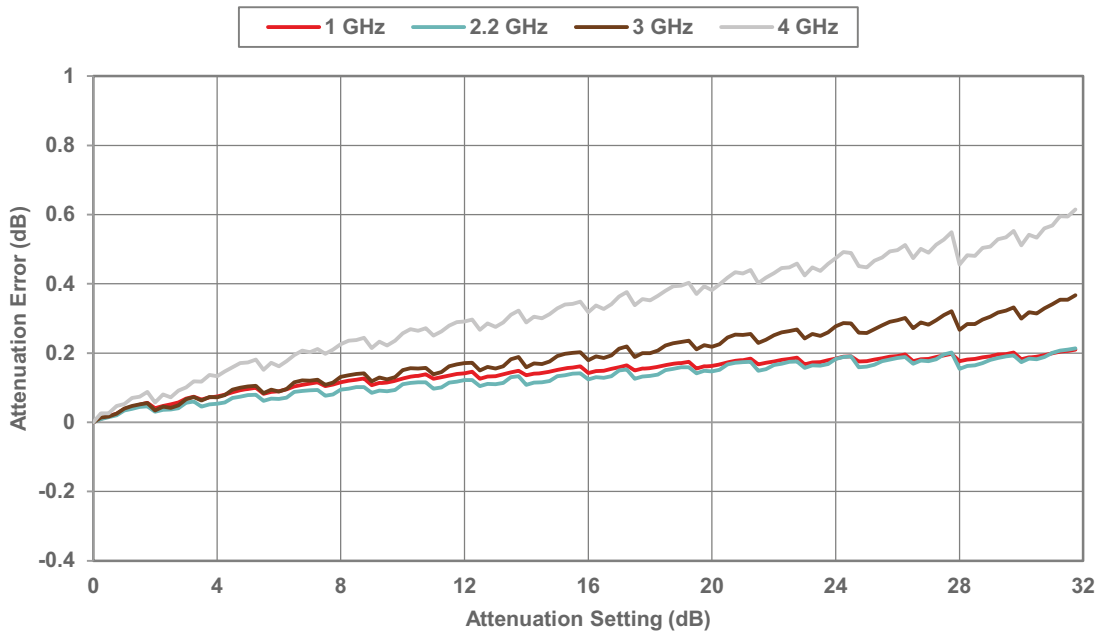
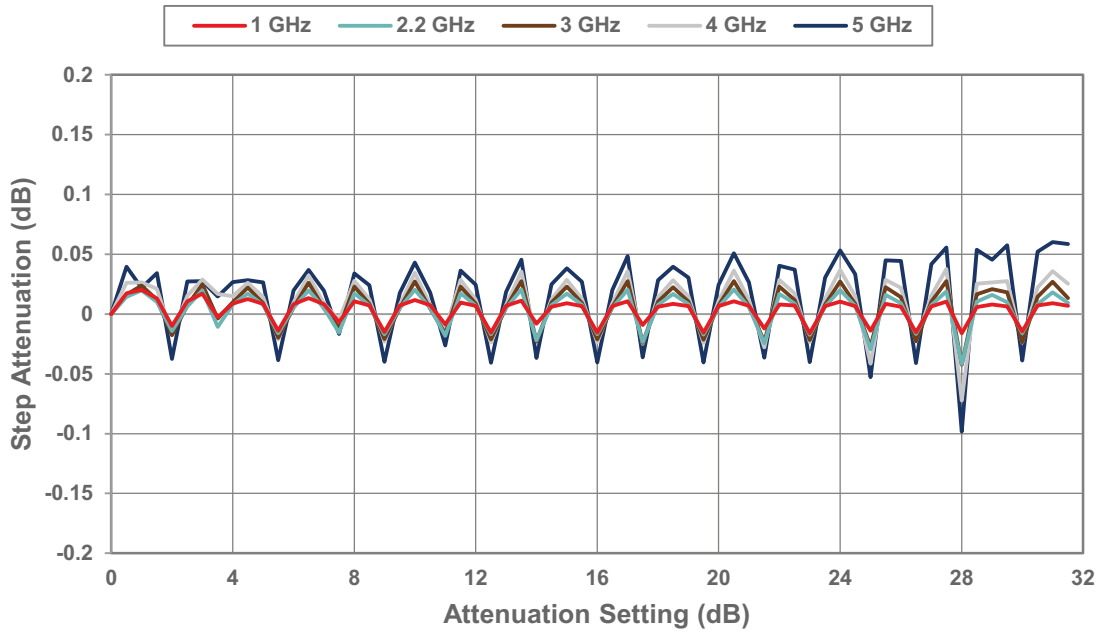


Figure 23 • 0.5-dB step attenuation vs. frequency<sup>(\*)</sup>



Note: \* Monotonicity is held so long as step attenuation does not cross below -0.5 dB.

Figure 24 • 0.5-dB step, actual vs. frequency

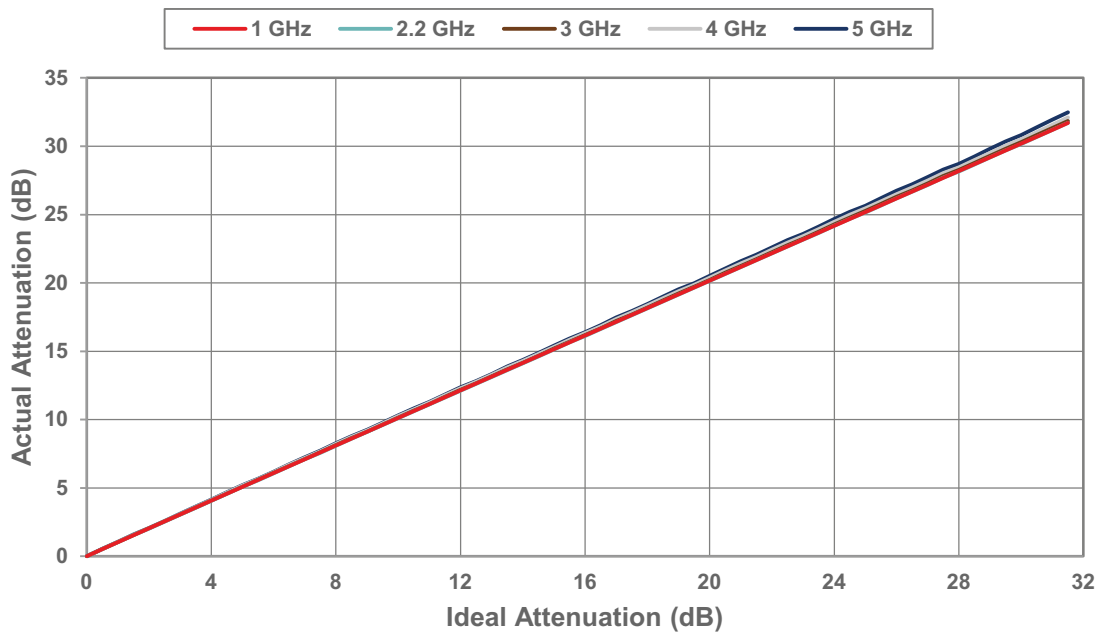


Figure 25 • 0.5 dB major state bit error vs. attenuation setting

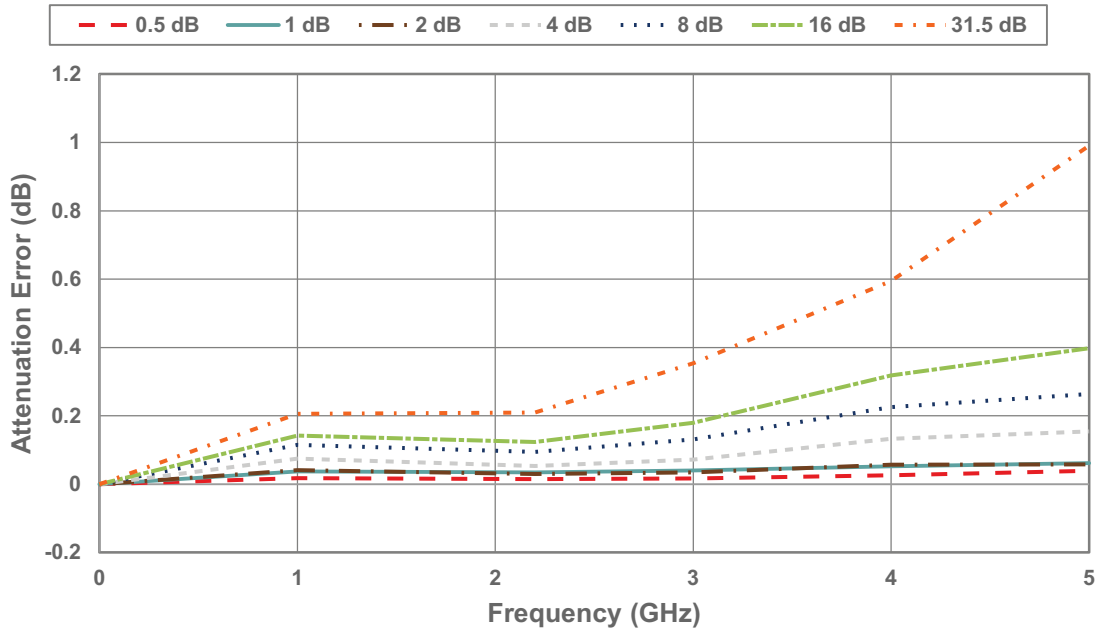


Figure 26 • 0.5 dB attenuation error vs. frequency

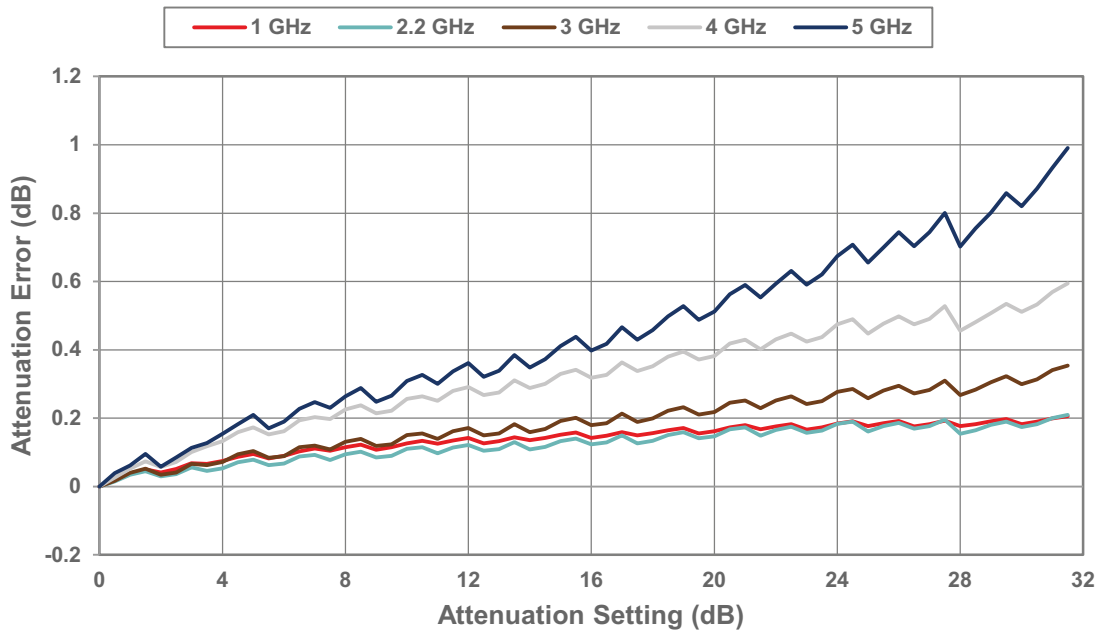
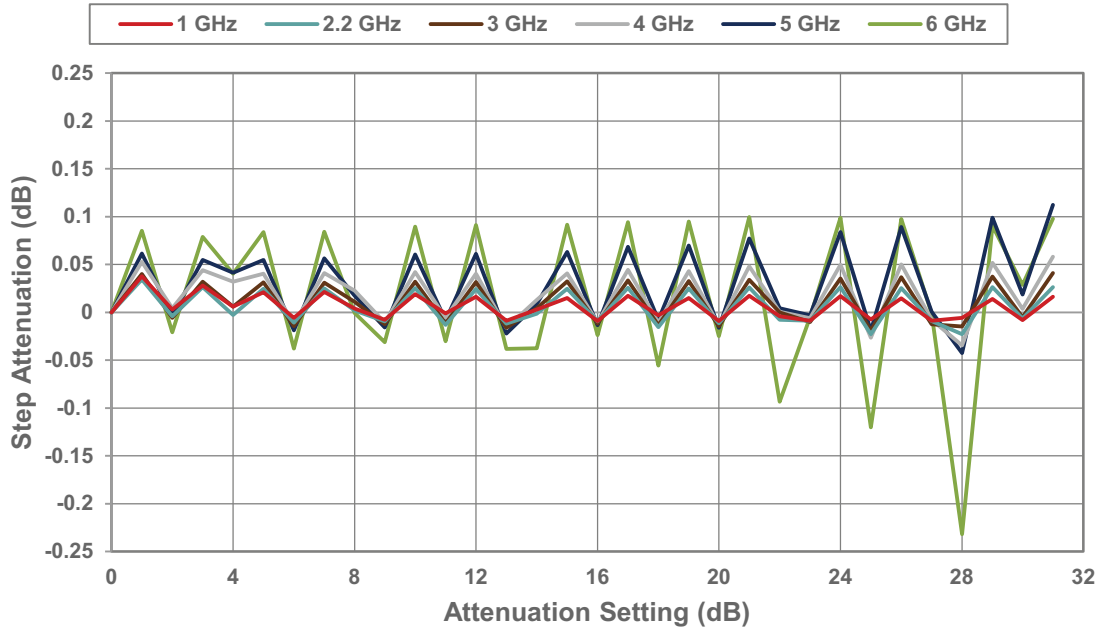


Figure 27 • 1-dB step attenuation vs. frequency(\*)



Note: \* Monotonicity is held so long as step attenuation does not cross below -1 dB.

Figure 28 • 1-dB step, actual vs. frequency

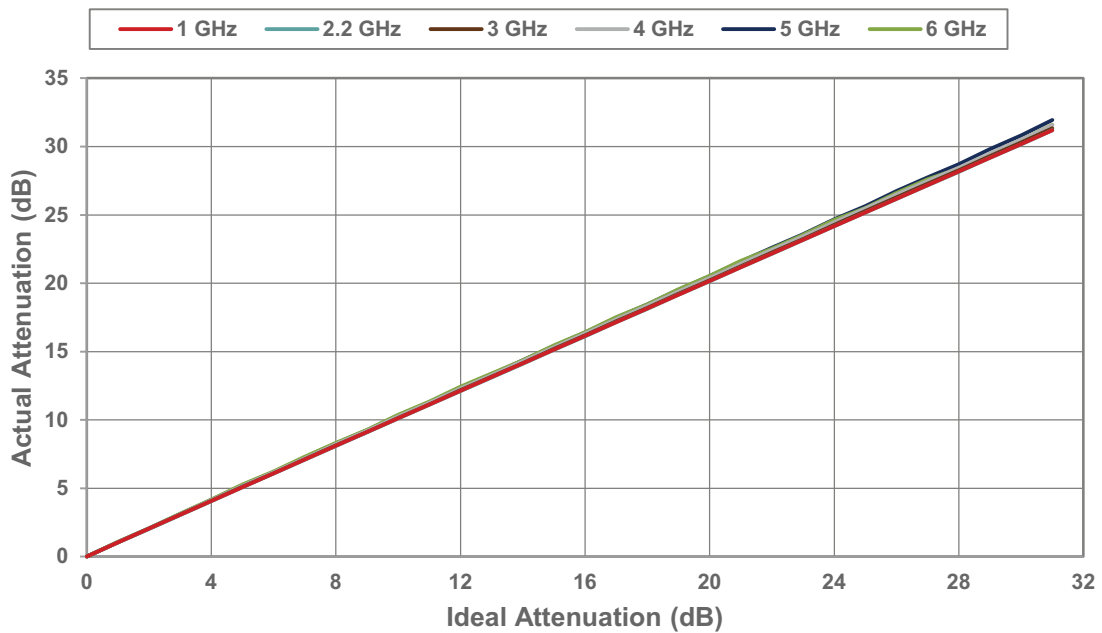


Figure 29 • 1 dB major state bit error vs. attenuation setting

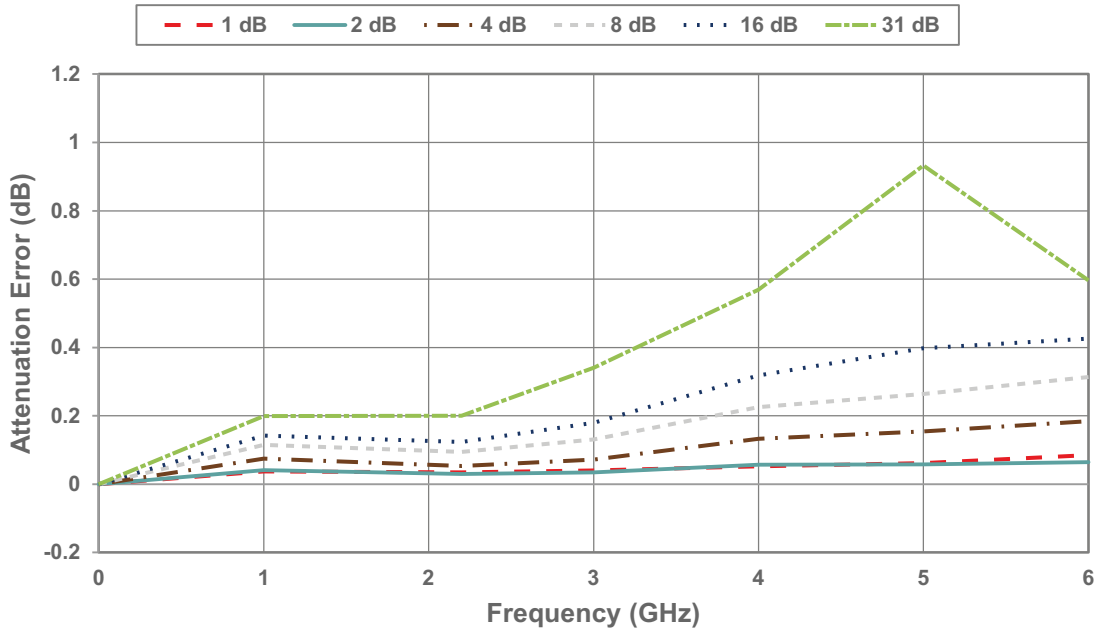


Figure 30 • 1 dB attenuation error vs. frequency

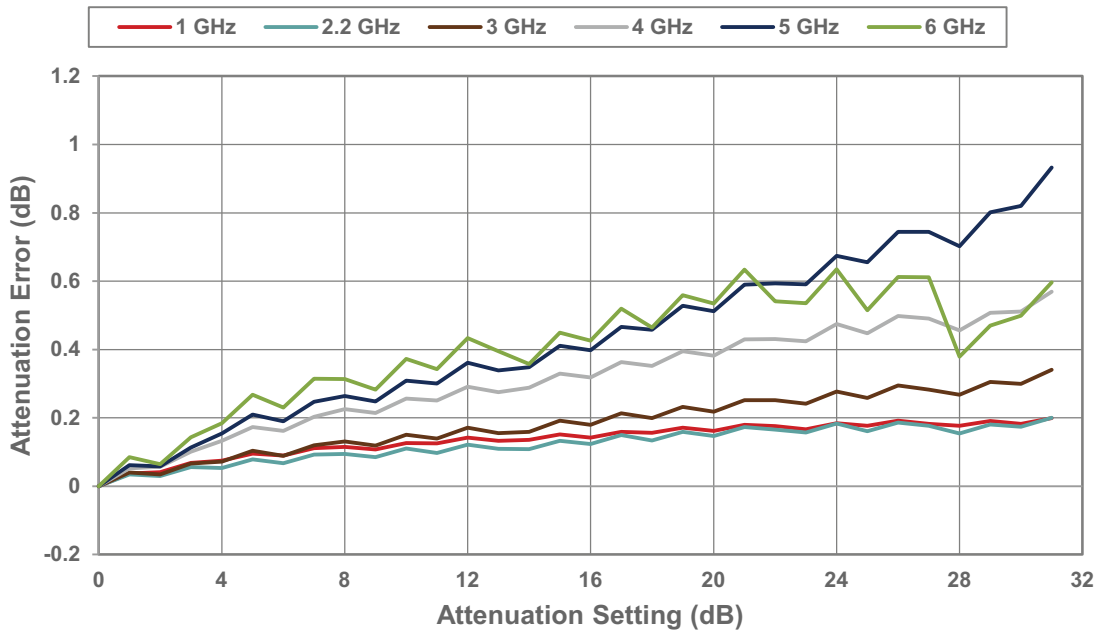


Figure 31 • Attenuation transient (15.75–16 dB), typical switching time = 275 ns

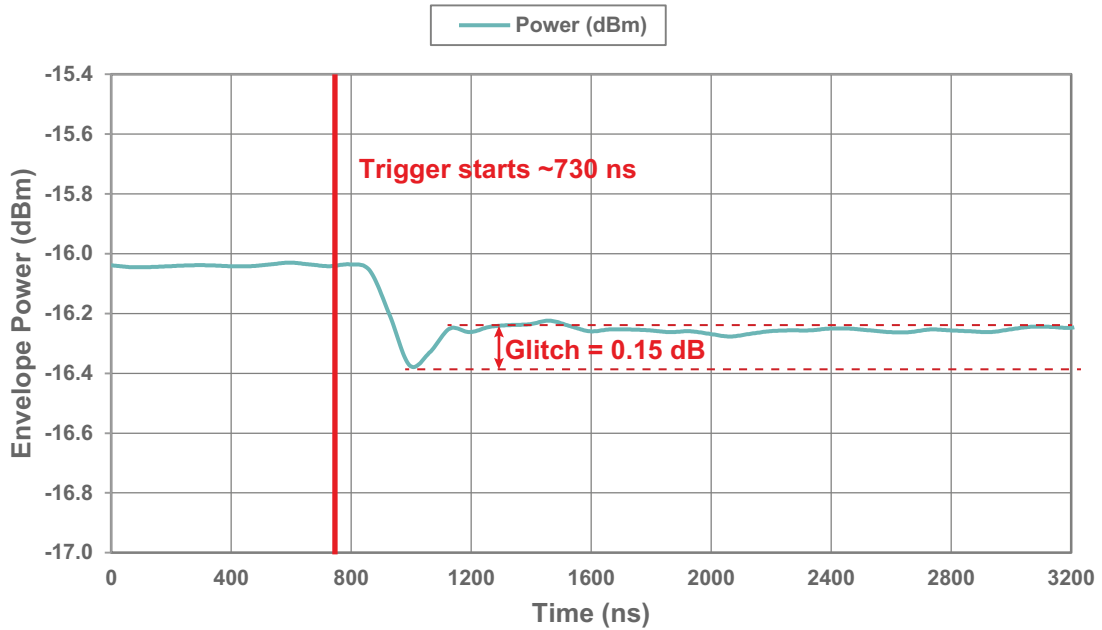
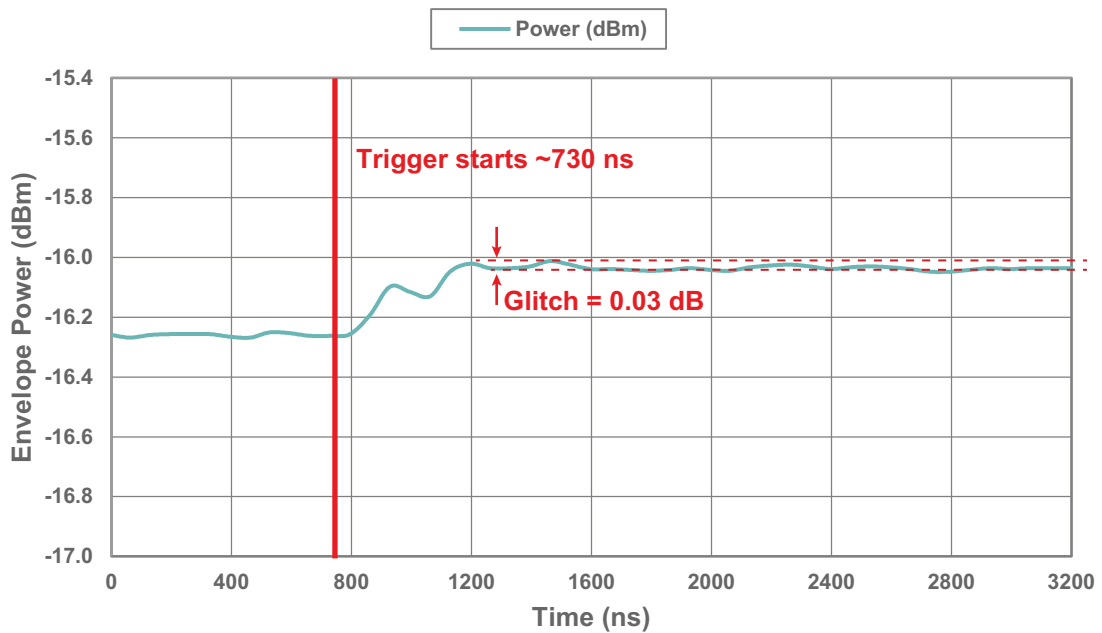


Figure 32 • Attenuation transient (16–15.75 dB), typical switching time = 275 ns



## Evaluation kit

pSemi designed the evaluation board (EVB) to ease your evaluation of the PE43713 DSA. The PE43713 EVB supports direct parallel, latched parallel, and serial modes.

### Evaluation kit setup

Connect the EVB with the USB dongle board and USB cable as shown in **Figure 33**.

### Direct parallel programming procedure

Direct parallel programming is suitable for manual operation without software programming. For manual direct parallel programming, position the Parallel/Serial (P/S) select switch to the Parallel position. The LE switch must be switched to HIGH position. Switches D0–D6 are SP3T switches that you can use to manually program the parallel bits. When D0–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting LE and D0–D6 to the EXT position presents as OPEN, which is set for software programming of the latched parallel and serial modes. **Table 4** lists the parallel truth table.

### Latched parallel programming procedure

For automated latched parallel programming, connect the USB dongle board and cable provided with the evaluation kit (EVK) from the USB port of the PC to the J5 header of the PE43713 EVB, and set the LE and D0–D6 SP3T switches to the EXT position. Position the Parallel/Serial (P/S) select switch to the Parallel position. The evaluation software is written to operate the DSA in parallel mode. Verify that the software GUI is set to latched parallel mode. Use the software GUI to enable the preferred attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

### Serial-addressable programming procedure

For automated serial programming, connect the USB dongle board and cable provided with the EVK from the USB port of the PC to the J5 header of the PE43713 EVB, and set the LE and D0–D6 SP3T switches to the EXT position. Position the Parallel/Serial (P/S) select switch to the Serial position. Before programming, define an address setting using the HDR2 header pin. Jump the middle column of pins on the HDR2 header (A0–A2) to the left column of pins to set logic LOW, or jump the middle row of pins to the right column of pins to set logic HIGH. If the HDR2 pins are left open, 000 becomes the default address. The software GUI is written to operate the DSA in serial mode. Use the software GUI to enable each setting to the preferred attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

*Figure 33 • PE43713 evaluation kit*

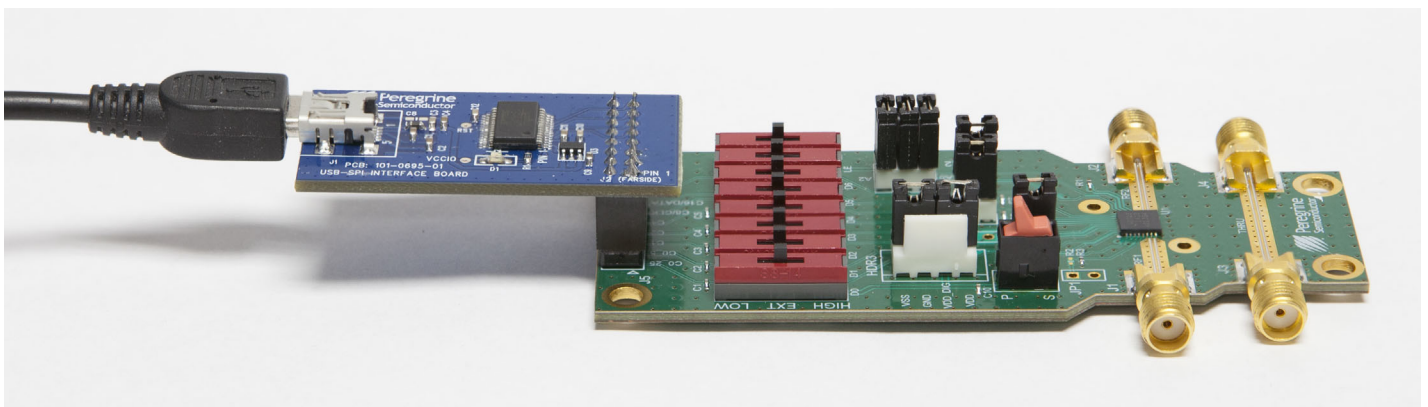
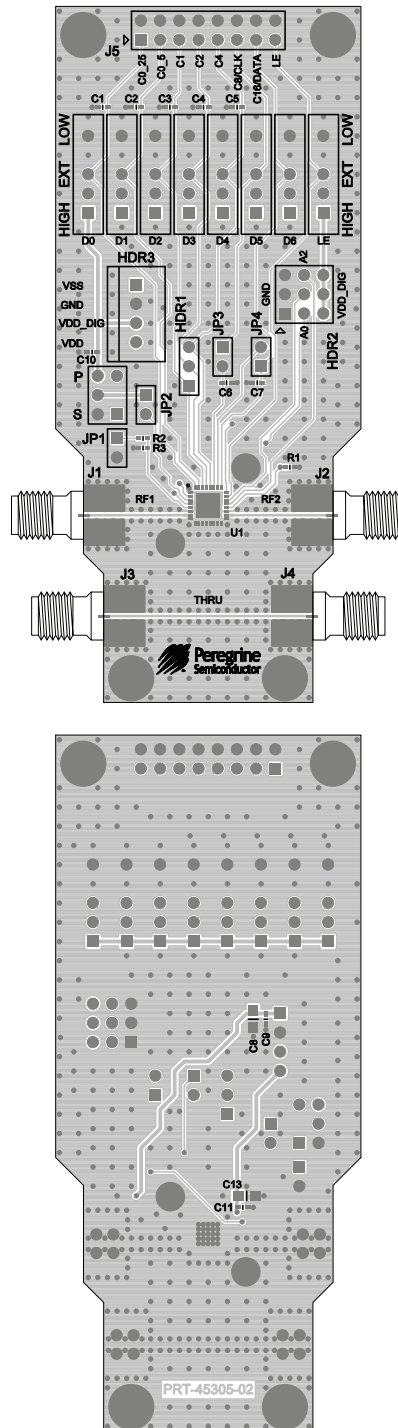


Figure 34 • PE43713 evaluation kit layout



## Pin information

Figure 35 shows the PE43713 pin map for the 32-lead 5 × 5 mm QFN package, and Table 10 lists the description for each pin.

Figure 35 • Pin configuration (top view)

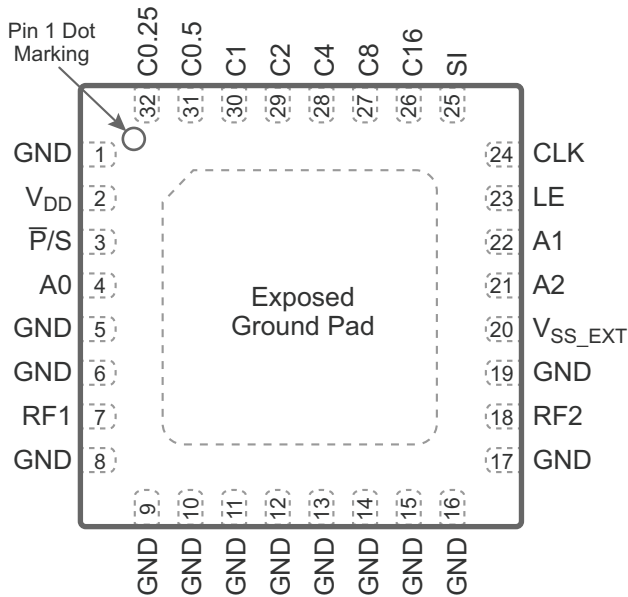


Table 10 • PE43713 pin descriptions

Pin no.	Pin name	Description
1, 5, 6, 8–17, 19	GND	Ground
2	V <sub>DD</sub>	Supply voltage
3	P/S	Serial/parallel mode select
4	A0	Address bit A0 connection
7 <sup>(1)</sup>	RF1	RF port 1 (RF input)
18 <sup>(1)</sup>	RF2	RF port 2 (RF output)
20 <sup>(2)</sup>	V <sub>SS_EXT</sub>	External V <sub>SS</sub> negative voltage control
21	A2	Address bit A2 connection
22	A1	Address bit A1 connection
23	LE	Serial interface Latch Enable input
24	CLK	Serial interface clock input
25	SI	Serial interface data input
26 <sup>(3)</sup>	C16 (D6)	Parallel control bit, 16 dB
27 <sup>(3)</sup>	C8 (D5)	Parallel control bit, 8 dB
28 <sup>(3)</sup>	C4 (D4)	Parallel control bit, 4 dB
29 <sup>(3)</sup>	C2 (D3)	Parallel control bit, 2 dB
30 <sup>(3)</sup>	C1 (D2)	Parallel control bit, 1 dB
31 <sup>(3)</sup>	C0.5 (D1)	Parallel control bit, 0.5 dB
32 <sup>(3)</sup>	C0.25 (D0)	Parallel control bit, 0.25 dB
Pad	GND	Exposed pad. Ground for proper operation.

**Notes:**

- 1) RF pins 7 and 18 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
- 2) Use V<sub>SS\_EXT</sub> (pin 20) to bypass and disable the internal negative voltage generator. Connect V<sub>SS\_EXT</sub> (pin 20) to GND (V<sub>SS\_EXT</sub> = 0V) to enable the internal negative voltage generator.
- 3) Ground C0.25, C0.5, C1, C2, C4, C8, and C16 if not in use.

## Packaging information

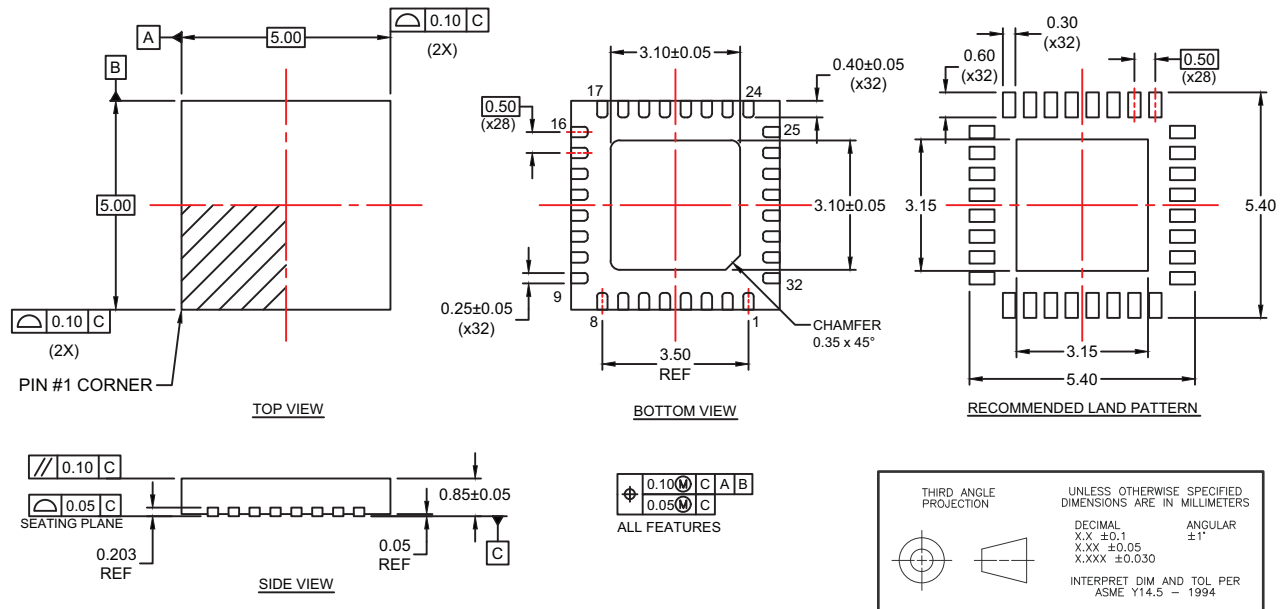
This section provides the PE43713 packaging data, including the moisture sensitivity level, package drawing, package marking, and tape-and-reel information.

### Moisture sensitivity level

The PE43713 moisture sensitivity level rating in the 32-lead 5 × 5 mm QFN package is MSL1.

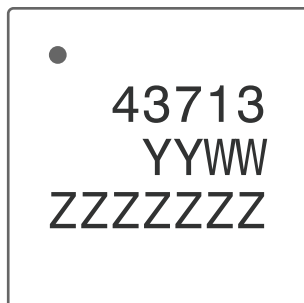
### Package drawing

Figure 36 • Mechanical drawing for the 32-lead 5 × 5 × 0.85 mm QFN package



### Top-marking specification

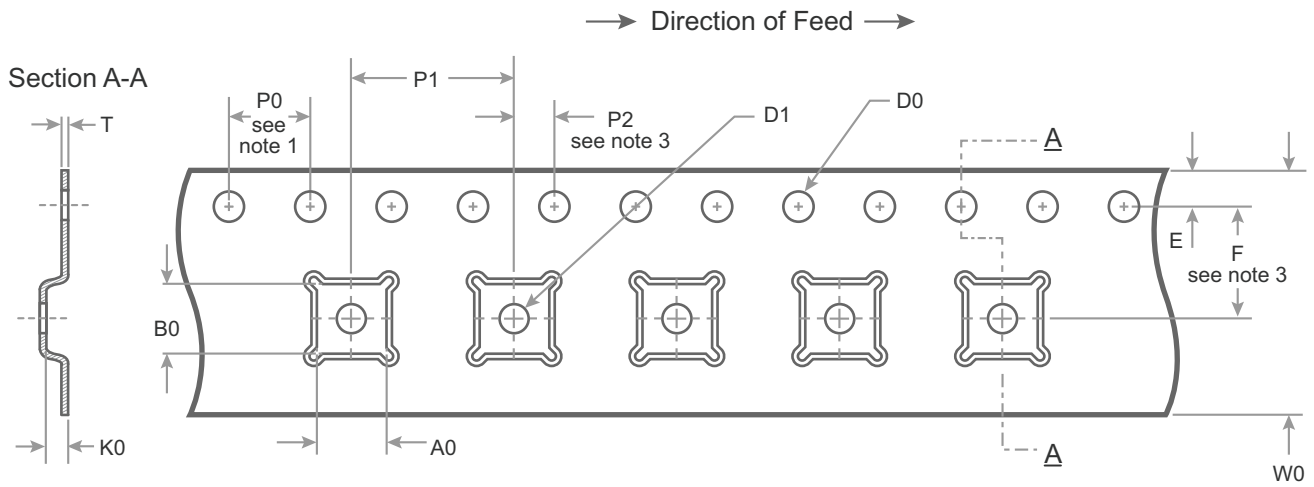
Figure 37 • PE43713 package marking specification



- = Pin 1 indicator
- YY = Last two digits of assembly year
- WW = Assembly work week
- ZZZZZZZ = Assembly lot code (maximum seven characters)

### Tape and reel specification

Figure 38 • Tape and reel specification for the 32-lead 5 × 5 × 0.85 mm QFN package

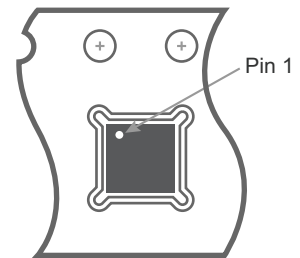


A0	5.25
B0	5.25
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

**Notes:**

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

## Ordering information

Table 11 • PE43713 order codes and shipping methods

Order code	Description	Packaging	Shipping method
PE43713A-Z	PE43713 Digital Step Attenuator	Green 32-lead 5 × 5 mm QFN	3000 units/T&R
PE43713B-Z	PE43713 Digital Step Attenuator	Green 32-lead 5 × 5 mm QFN	3000 units/T&R
EK43713-02	PE43713 Evaluation Kit	Evaluation kit	1/box
EK43713-03	PE43713 Evaluation Kit	Evaluation kit	1/box

## Document Categories

### Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

### Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

### Product Brief

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