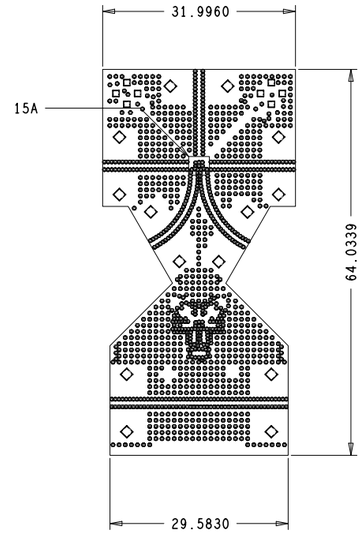
DWG NO.	SH	REV
PRT-80043	1	01

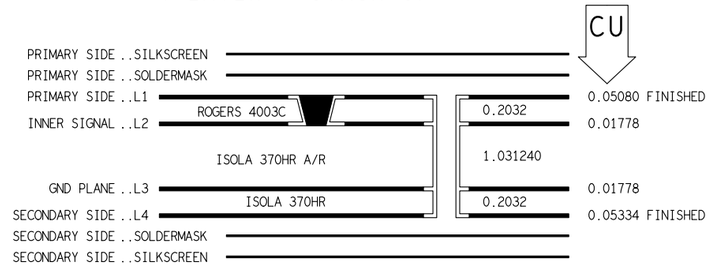
NOTES: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN METRIC

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. ~~GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES, REMOVE PRIOR TO FABRICATION.~~
3. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2.
   THE DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS.
   BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.
4. TRACE WIDTH/SPACE/VIA:
   TRACE WIDTHS/SPACING TO BE WITHIN ±20% OF GERBER DATA.
   MINIMUM TRACE WIDTH: OUTER LAYERS= 0.127mm ±10%.
   INNER LAYERS= NA ±20%.
   MINIMUM AIR GAP: OUTER LAYERS= 0.1016 ±20%.
   INNER LAYERS= NA ±20%.
   MINIMUM VIA PAD DIAMETER: 0.20mm ±20%.
5. MATERIAL:
   NUMBER OF ELECTRICAL LAYERS IS 4
   MATERIALS AND OVERALL THICKNESS SEE STACKUP DETAIL.
   LOAD BOARD AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.
   MATERIAL'S GLASS TRANSITION TEMPERATURE (Tg) SHALL BE A MINIMUM OF
   170° CENTIGRADE.
   MATERIAL MUST MEET UL796 WITH A FLAMMABILITY RATING OF 94V-0
   VENDOR UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE. IF NO BOTTOM
   SILKSCREEN PROVIDED VENDOR MAY ADD BOTTOM SILKSCREEN.
6. TOLERANCES:
   6A. LAYER TO LAYER REGISTRATION WITHIN .076mm.
   6B. ALL HOLES TO BE LOCATED WITHIN .076mm OF ORIGINAL CAD DATA.
   6C. ALL HOLES SURROUNDED BY COPPER SHALL HAVE A MINIMUM ANNULAR RING OF .076mm.
   6D. ALL PLATED THROUGH HOLES TO HAVE A MINIMUM .025mm OF PLATING.
   6E. HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.
   6F. WARP AND TWIST NOT TO EXCEED .254 MM/MM.
   6G. CONDUCTOR WIDTHS/SPACINGS TO BE WITHIN ±20% OF GEBER DATA.
   ~~6H. EDGE PLATING REQUIRED AT CONNECTOR GND PINS AS OUTLINED ON SHEET 2 DETAILS 'A', 'B', & 'C'.~~
7. PLATING OPTIONS: USE 7A
   7A. IAg - IMMERSION SILVER 30-50 MICROINCHES PER IPC-4553.
   ~~7B. 0.05 UM OVER ELECTROLESS PALLADIUM OVER 2-5 UM OF PALLADIUM PER IPC-4552.~~
   ~~7D. SELECTIVE HARD GOLD FINISH IN THE BUT AND FINGER AREA(S), PLATED 1.50-100 MICROINCHES MICROINCHES THICK (KNOOP HARDNESS 130-200) OVER NICKEL PLATE IN ACCORDANCE WITH IPC-4-600, LATEST REVISION, SECTION 1.0, CLASS 3 (200-800 MICROINCHES THICK). FABRICATE IN ACCORDANCE WITH IPC-6012, START WITH 1/2 OZ. COPPER.~~
   ~~7G. HASL (HOT AIR SOLDER LEVEL) SMT PADS MUST BE FLAT TO A MAX OF .076mm (.003") ABOVE SURFACE. HASL FINISH TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH ROHS DIRECTIVES.~~
8. APPLY LPI (LIQUID PROTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840
   CLASS "T" TO TOP SIDE OF PCB. SOLDERMASK COLOR TO BE: GREEN
   GERBER FILES REFLECT A ZERO OVERSIZE. VENDOR MAY OVERSIZE AS NEEDED, MAX THICKNESS
   .020mm. ~~IT IS NOT ACCEPTABLE FOR SOLDERMASK WEDDING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.~~
9. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL
   EXPOSED COPPER. TOP SIDE.
10. VENDOR TO REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS.
11. VENDOR MAY ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.
12. REMOVE ALL BURRS AND BREAK SHARP EDGES, INSIDE CORNER MAXIMUM RADIUS 381mm.
13. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST "PRT-80043-01.IPC".
14. MATRIX DRAWING: USE 14A
    14A. NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.
    ~~14B. MATRIX DRAWING PROVIDED, SEE FABRICATION DRAWING SHEET 2 OF 2.~~
    ~~14C. VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY PSEMI. PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK AWAY TABS. SEE DETAIL B. SUPPORT RAIL WIDTH TO BE 6.35mm + 12.7mm WITH 1.52mm FIDUCIALS AND 3.175mm TOOLING HOLES IN 3 CORNERS. PANELIZED SOLDERPASTE GERBER TO BE SUBMITTED TO PSEMI.~~
15. PLANARITY: USE 15A,15B.
    15A. VARIATION OF BUMP PADS IN THE Z AXIS TO BE <=5um.
    15B. ALL VIAS TO BE NON-CONDUCTIVE EPOXY FILLED AND COPPER OVERPLATED AFTER PLATING AND BEFORE FINAL SURFACE FINISH. NON-CONDUCTIVE EPOXY (SAN_EI 900 OR EQUIVALENT) IS RECOMMENDED. EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES. A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.
    ~~15C. ALL OTHER VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.~~
16. CONTROLLED IMPEDANCE REQUIREMENTS: USE 16B
    VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM PSEMI.
    ~~16A. NO CONTROLLED IMPEDANCE MEASUREMENTS REQUIRED.~~
    16B. VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.
    0.3556mm TRACES ON LAYER 1 ARE 50 OHMS, TRANSMISSION LINES X +/-5%.
    ~~+XXmm (+XXmil) TRACES ON LAYER Y ARE 50 OHMS, MICROSTRIP, +/- 10%.~~
    ~~+XXmm (+XXmil) TRACES ON LAYER Y ARE 100 OHMS, DIFFERENTIAL, +/- 10%.~~
17. SHORTS DESIGNED IN BOARD: NO
    ~~NET XXXXXXXXXXXX.~~
    ~~NET XXXXXXX TO GND, LAYER X~~
18. IPC-2221 TEST COUPONS A & B REQUIRED. TEST COUPONS SHALL BE IDENTIFIED AND TRACEABLE TO THE LOT. TEST COUPONS, DATA, CROSSECTIONS VERIFYING WIDTH AND CERTIFICATES OF CONFORMANCE SHALL ACCOMPANY ALL SHIPMENTS. MATERIAL VERIFICATION SHALL ALSO BE SENT IN WRITING. SHIPMENTS WITHOUT THESE CERTIFICATIONS WILL NOT BE ACCEPTED.
19. DEVIATIONS BY FABRICATION FACILITY TO BE REPORTED TO PSEMI.



REVISIONS				
ZONE	REV		APPROVALS	DATE
	01		R.ALIDIO	06/30/21

4 LAYER - STACK UP



TOTAL BOARD THICKNESS: 1.5748 ±0.127
UNITS: Metric

DRILL CHART: TOP to LAYER_2

ALL UNITS ARE IN MILLIMETERS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
○	0.3	+0.0/-0.3	PLATED	148

TOTAL HOLES: 148

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILLIMETERS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
○	0.3	+0.0/-0.3	PLATED	1062
□	1.0	+0.075/-0.075	PLATED	8
◇	2.0	+0.075/-0.075	PLATED	14

TOTAL HOLES: 1084

DIMENSIONS IN mm/[Inches]
TOLERANCES UNLESS OTHERWISE NOTED
X.X ± +/- .2.5/[.1]
X.XX ± +/- .25/[.01]
X.XXX ± +/- .127/[.005]
X.XXXX ± +/- .0127/[.0005]
ANGLES ± +/- 1/2 DEG

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN R.MARROQUIN	06/30/21
CHECKED R.ALIDIO	06/30/21
ISSUED	
REVISIED BY	

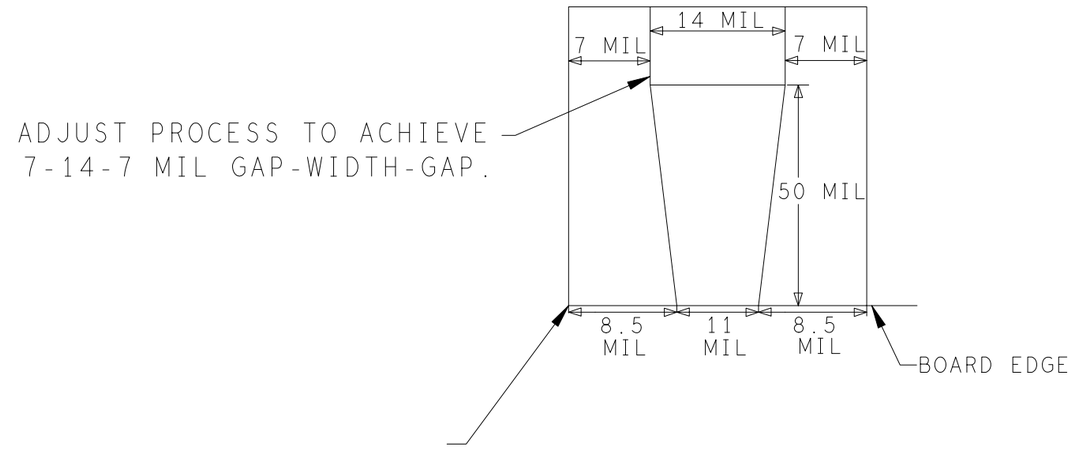
COMPANY pSemi™ A Murata Company
9380 Carroll Park Drive
San Diego, CA, 92121
(858)731-9400 Phone
(858)731-9499 Fax

TITLE
PCB,
PE42546 Shaggy EVK Board

SIZE	RoHS COMPLIANCE RELEASE DATE	DWG NO.	REV
B	Pb	PRT-80043	01

SCALE: NONE SHEET: 1 OF 2

DETAIL C



ADJUST PROCESS TO ACHIEVE 7-14-7 MIL GAP-WIDTH-GAP.

A TAPERED LINE IS USED FOR CONNECTOR TRANSITION. ADJUST PROCESS TO ACHIEVE 8.5-11-8.5 MIL GAP-WIDTH-GAP.