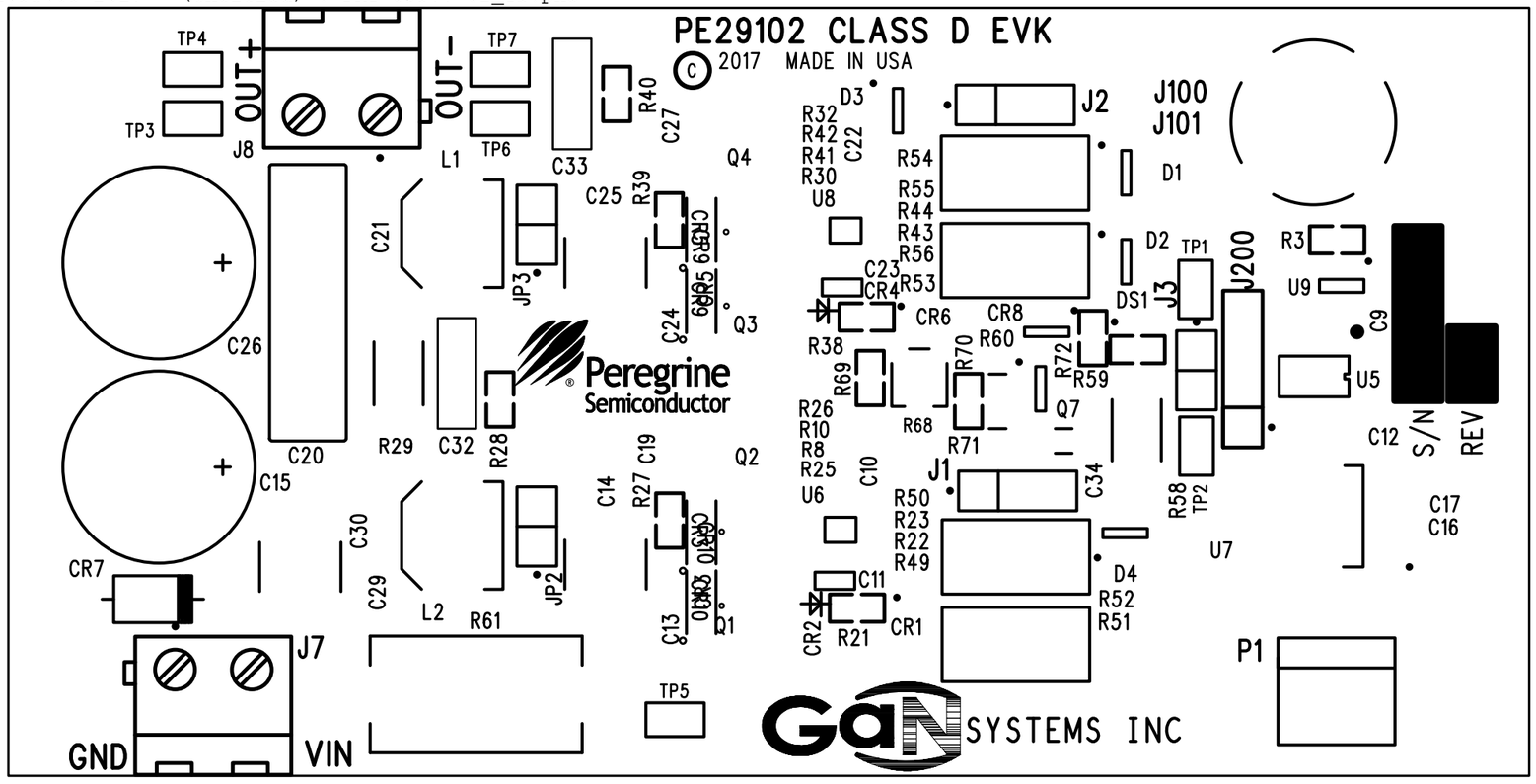

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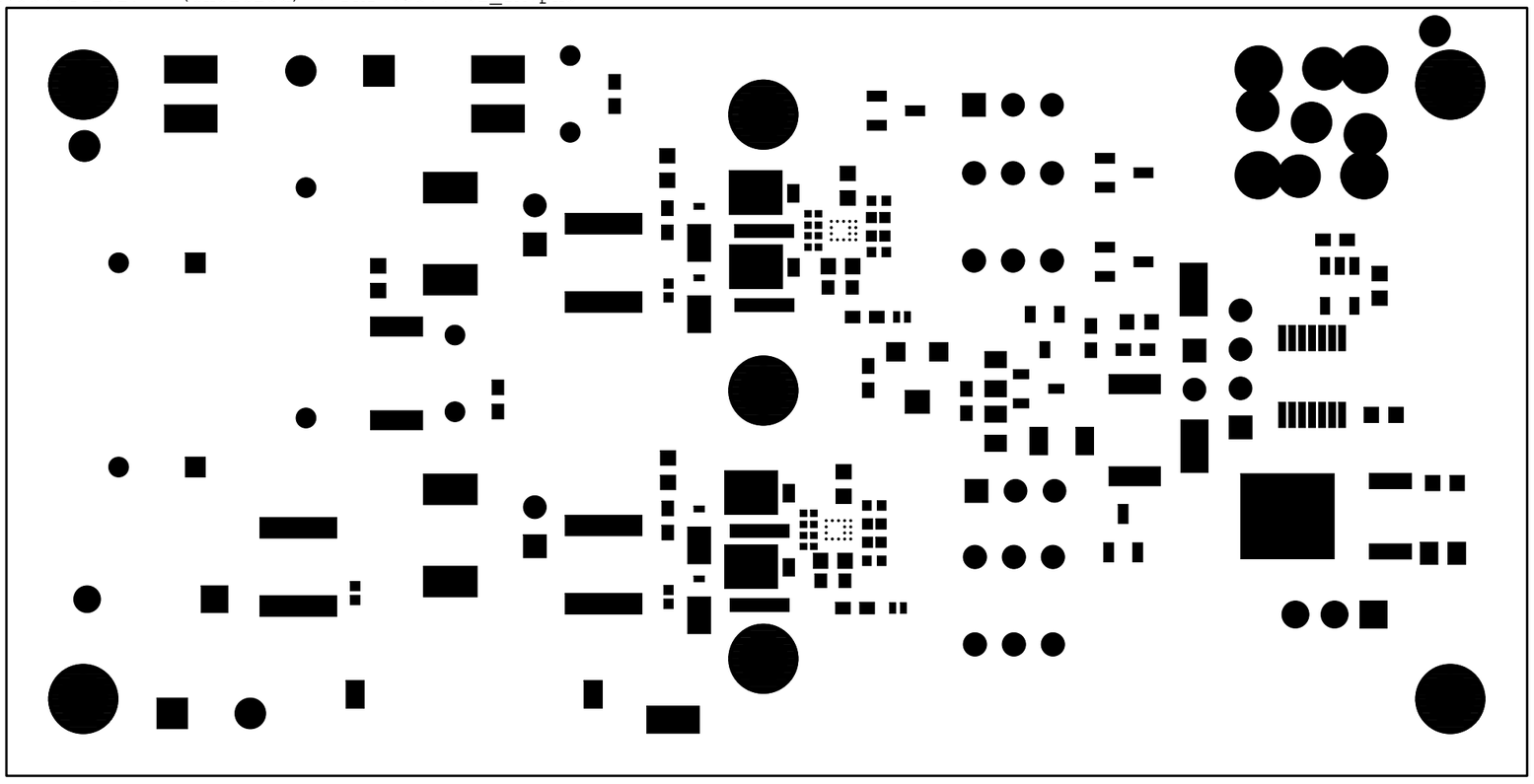
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: SILKSCREEN (PRIMARY SIDE)			SHEET: 1 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	



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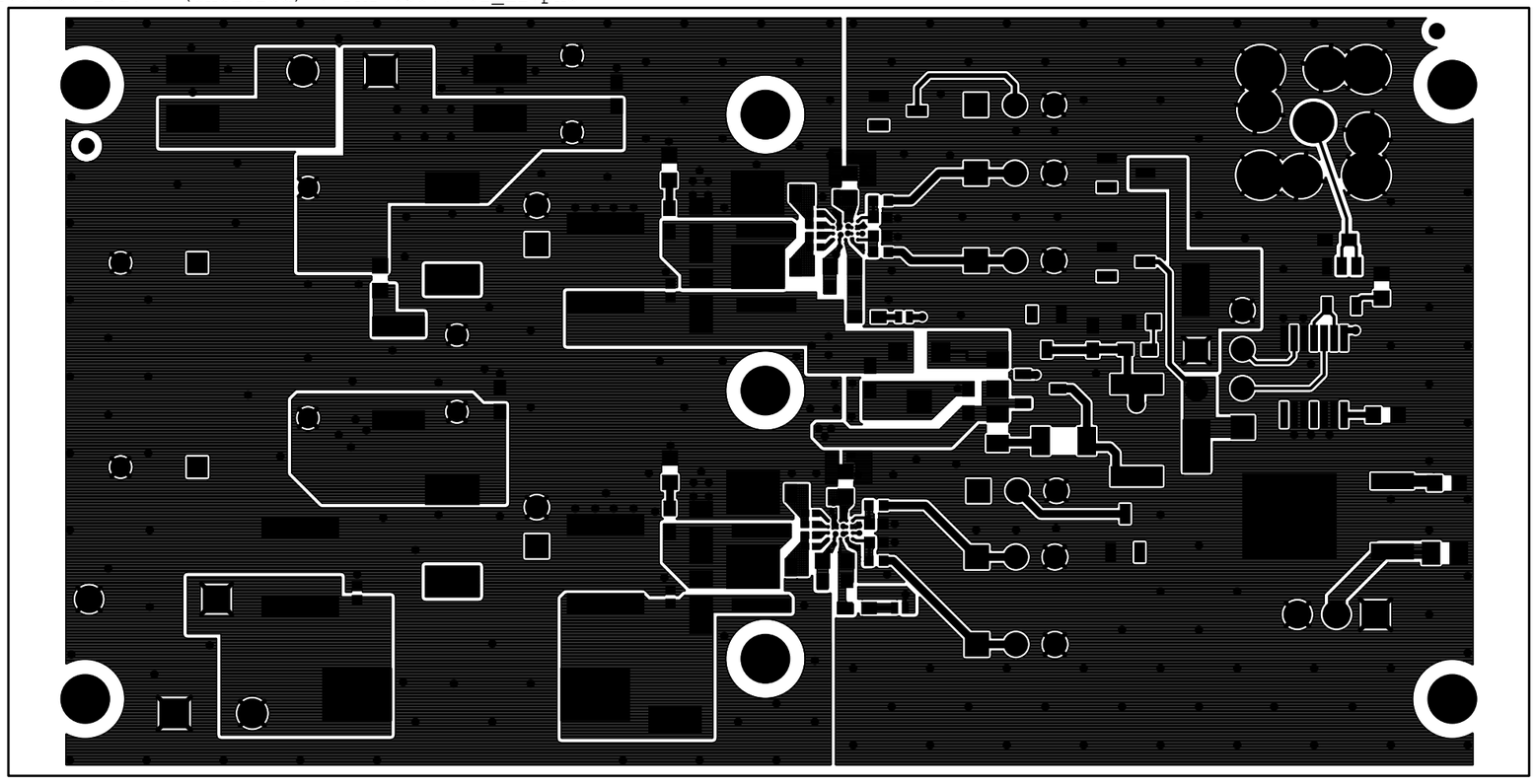
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: SOLDER MASK (PRIMARY SIDE)			SHEET: 2 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:03 2017 - (Untitled) : PRT-69377-02_L1.pho



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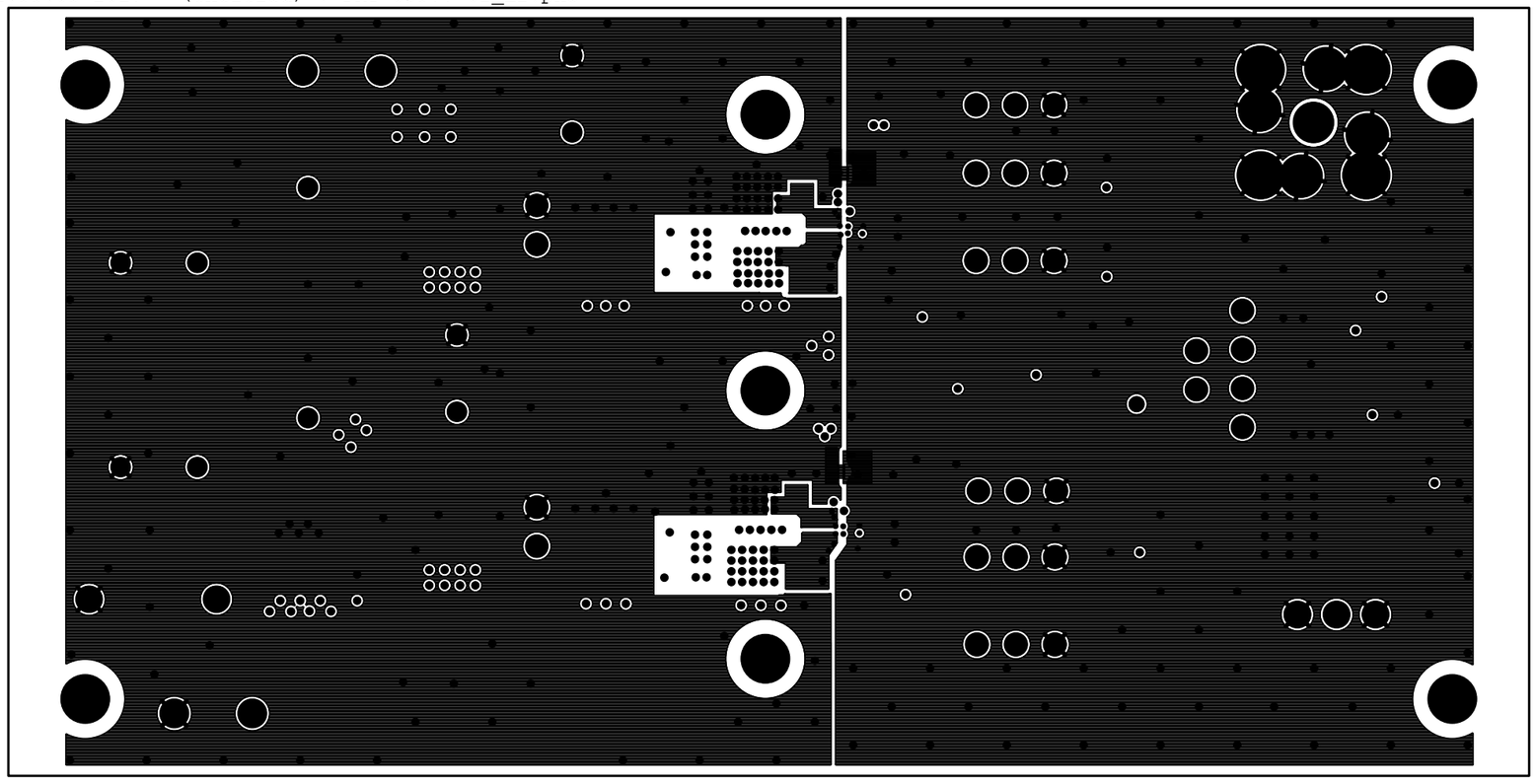
(858)731-9499 Fax

BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: LAYER 1 (PRIMARY SIDE)			SHEET: 3 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:03 2017 - (Untitled) : PRT-69377-02_L2.pho



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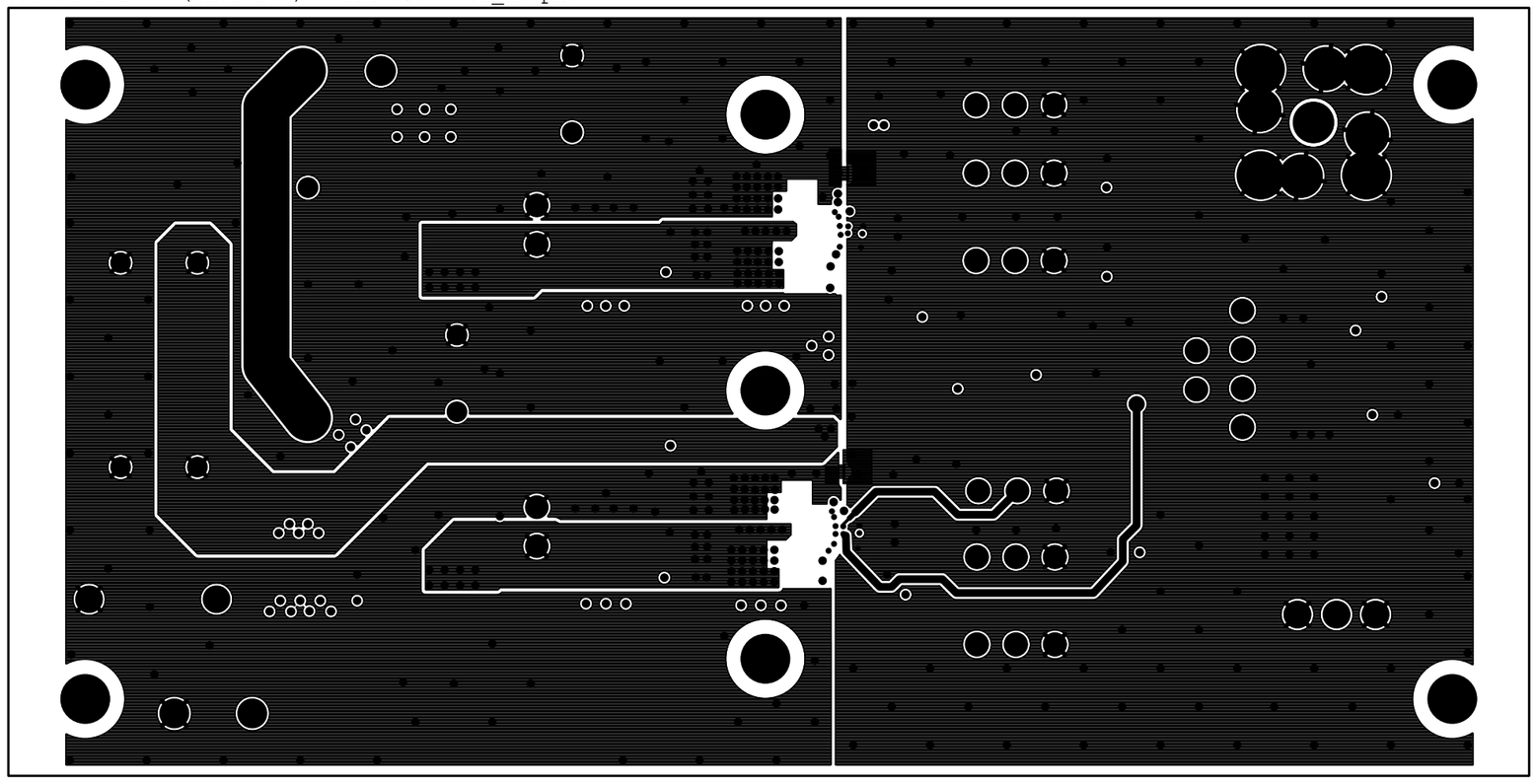
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: LAYER 2 (GND PLANE)			SHEET: 4 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:04 2017 - (Untitled) : PRT-69377-02_L3.pho



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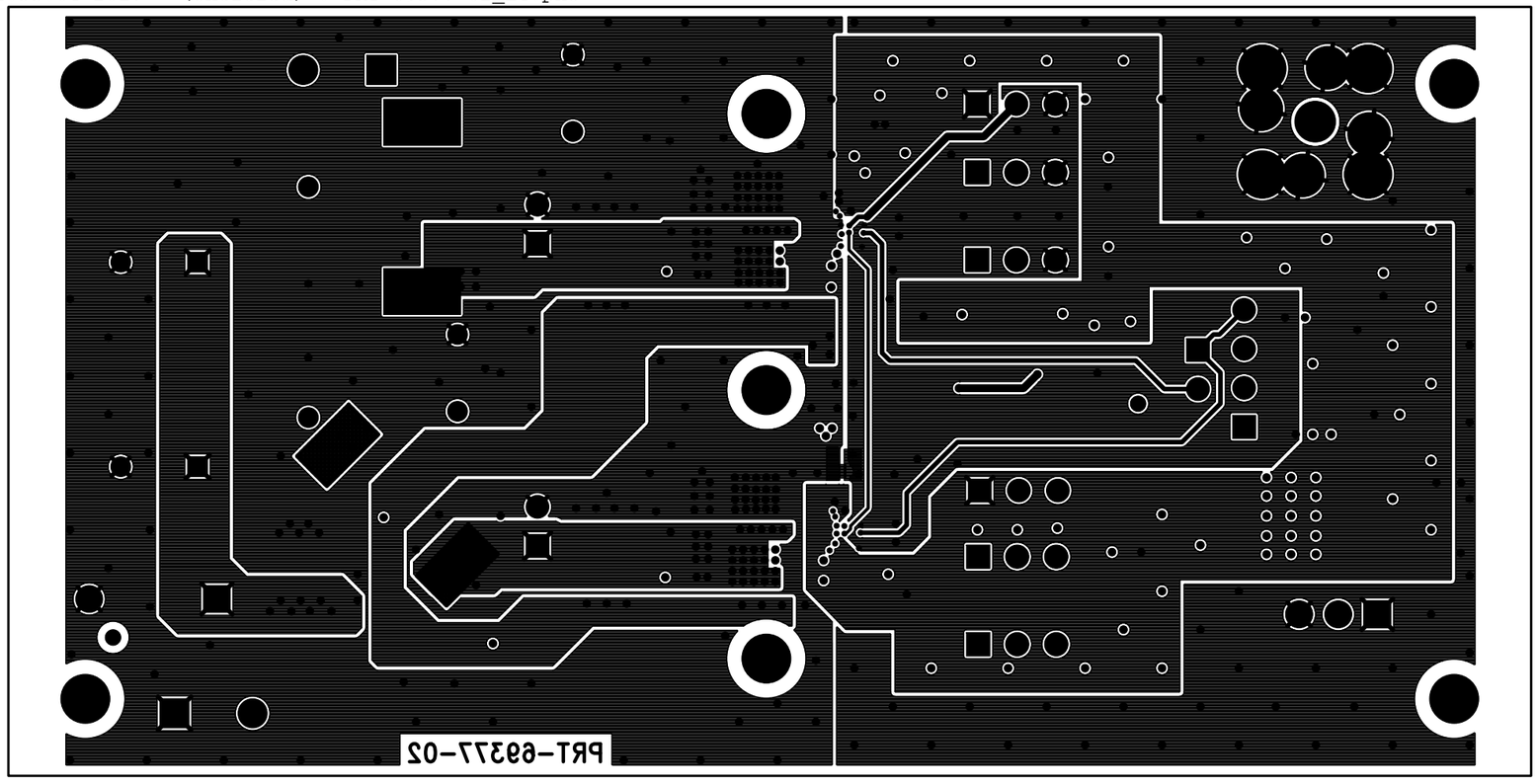
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: LAYER 3 (GND PLANE)			SHEET: 5 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	



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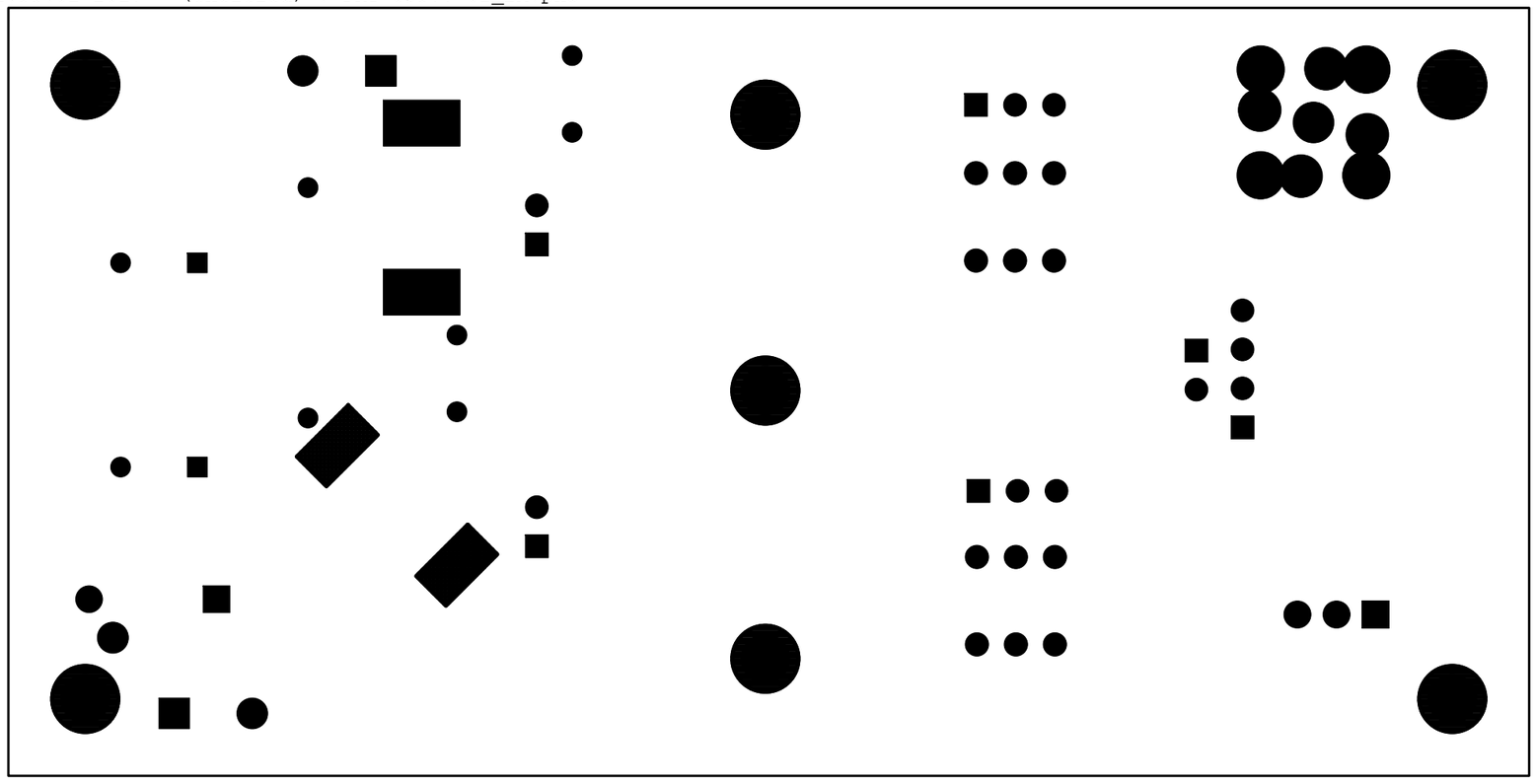
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: LAYER 4 (SECONDARY SIDE)			SHEET: 6 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:02 2017 - (Untitled) : PRT-69377-02_BM.pho



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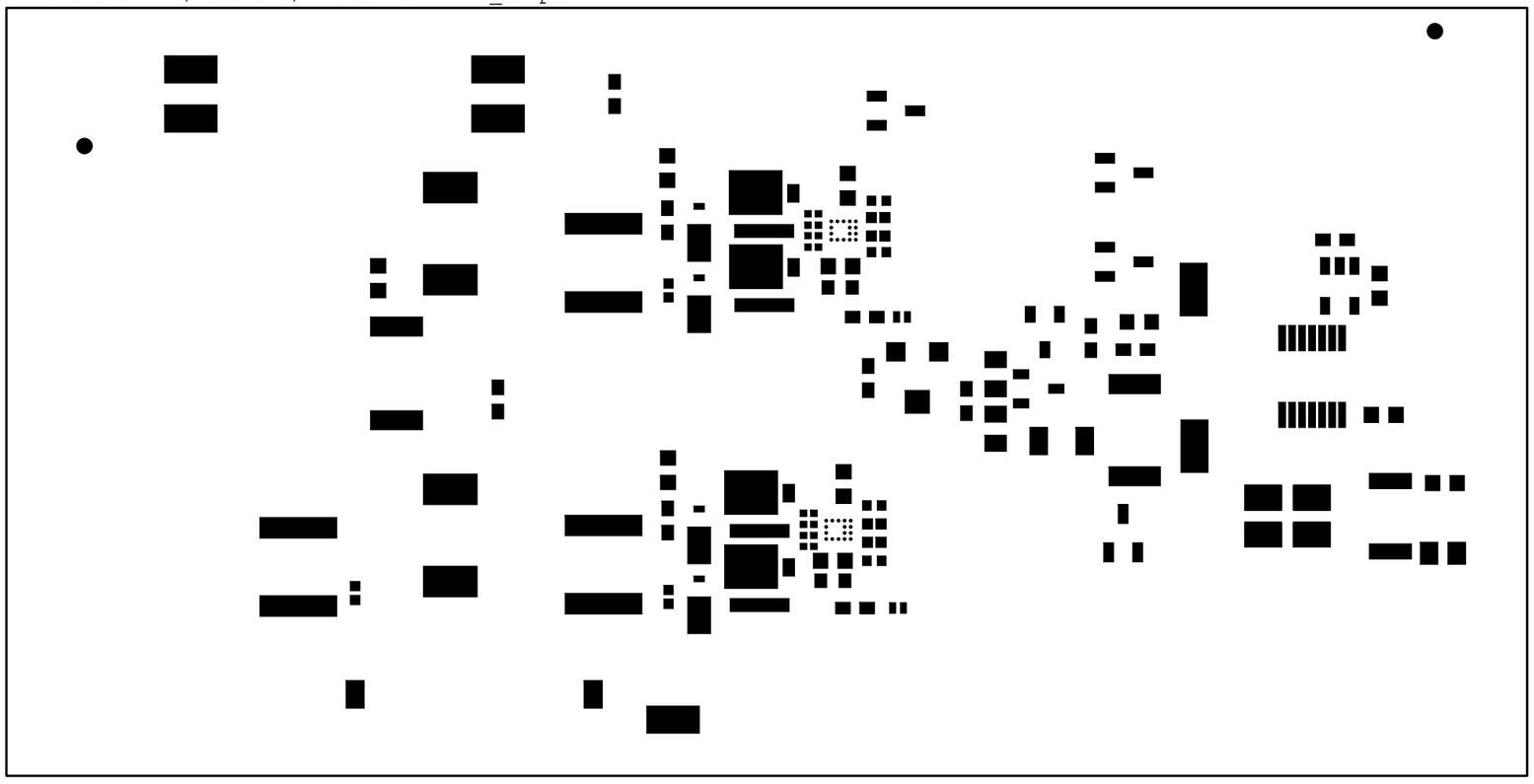
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: SOLDER MASK (SECONDARY SIDE)			SHEET: 7 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:04 2017 - (Untitled) : PRT-69377-02_TP.pho



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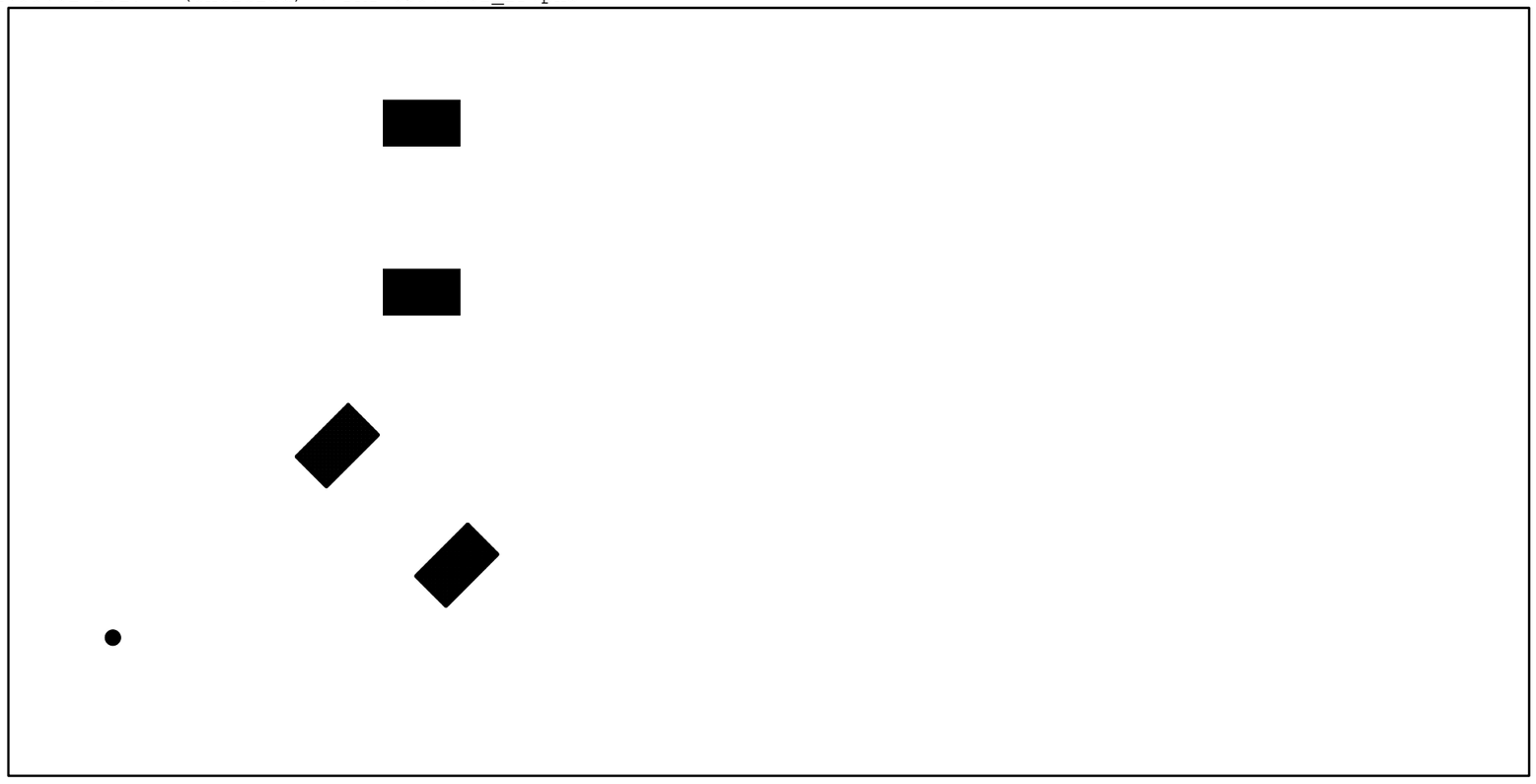
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: SOLDER PASTE (PRIMARY SIDE)			SHEET: 8 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:02 2017 - (Untitled) : PRT-69377-02_BP.pho



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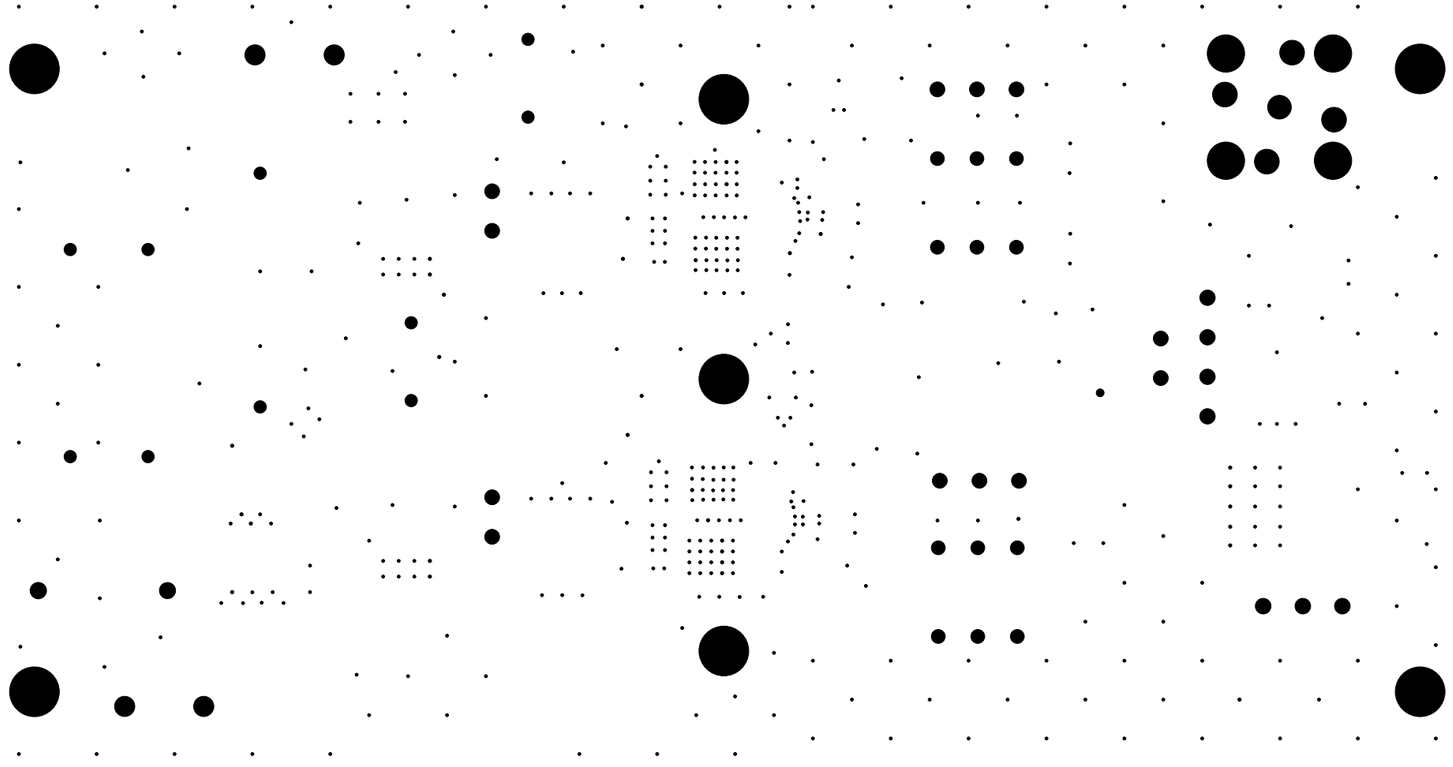
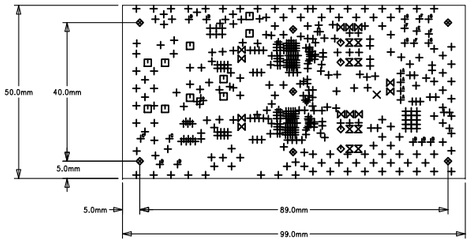
BOARD NAME: PE29102 CLASS D EVK			
PART NUMBER: PRT-69377			REV: 02
LAYER NAME: SOLDER PASTE (SECONDARY SIDE)			SHEET: 9 of 9
DATE: 09-11-17	SCHEMATIC: DOC-83239-02	DESIGNER: D. KENDRICK	

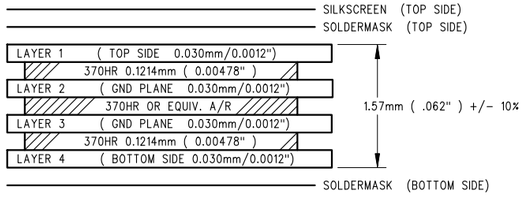
CAM350/DFMSTREAM V 12.1 : Mon Sep 11 14:35:05 2017 - (Untitled) : prt-69377-02_nc.drl



SIZE	QTY	SYM	PLATED	TOL
0.2032	472	+	YES	+/-0.2032
0.508	1	X	YES	+/-0.508
0.8	10	⊡	YES	+/-0.075
0.889	4	◇	YES	+/-0.075
0.9	8	⧖	YES	+/-0.075
0.9652	12	⋈	YES	+/-0.075
1	4	A	YES	+/-0.075
1.016	3	B	YES	+/-0.075
1.05	2	C	YES	+/-0.075
1.3	4	D	YES	+/-0.075
1.524	1	E	YES	+/-0.075
1.6002	4	F	YES	+/-0.075
2.4	4	G	YES	+/-0.075
3.2	7	◈	NO	+/-0.05



4 LAYER STACK-UP DETAIL



DWG NO.	SH	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

NOTES: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN METRIC

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES, REMOVE PRIOR TO FABRICATION.
3. FABRICATION VENDOR MAY ADD ___TEARDROPS, ___SOLDER TAILS TO PADS IN DUT AREA.
4. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2.
   THE DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS.
   BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.
5. NUMBER OF ELECTRICAL LAYERS IS "4". SEE LAYER STACKUP DETAIL FOR MATERIALS AND OVERALL THICKNESS.
   MINIMUM TRACE WIDTH FOR OUTER LAYERS = .20mm (.008") +/-20%, FOR INNER LAYERS = NA.
   MINIMUM AIR GAP FOR OUTER LAYERS = .14mm (.0055") +/-20%, FOR INNER LAYERS = .20mm (.008") +/-20%.
   MINIMUM VIA PAD DIAMETER = 0.3429mm (.0135") +/-20%.
   _X_ NOTE; THIS PCB HAS < .076mm (.003") TRACE/SPACE IN DUT AREA.
6. MATERIAL: LAMINATE AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.
   MINIMUM FINISHED EXTERNAL LAYER COPPER THICKNESS = _X_0.030mm(.0012"). ___0.046mm(.0018"). ___0.0508mm(.002")
   MINIMUM INTERNAL LAYER COPPER THICKNESS = ___0.0152(.0006"). _X_0.030mm(.0012").. ___0.0508mm(.002")
   THE MATERIAL'S GLASS TRANSITION TEMPERATURE (Tg) SHALL BE A MINIMUM OF 170 DEGREES CENTIGRADE.
   MATERIAL MUST MEET UL796 WITH A FLAMMABILITY RATING OF 94V-0
   VENDOR'S UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE.
7. LAYER TO LAYER REGISTRATION WITHIN .076 (.003"). ALL HOLES TO BE LOCATED WITHIN .076mm (.003") OF ORIGINAL CAD DATA.
   ALL HOLES SURROUNDED BY COPPER LAND SHALL HAVE A MINIMUM ANNULAR RING OF .076mm (.003").
   ALL PLATED THROUGH HOLES TO HAVE A MINIMUM .025mm (.001") OF PLATING.
   HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.
   ___ .XX (XXX") VIAS MAY HAVE AN ANNULAR RING OF ZERO
8. PLATING OPTIONS:
   _X_ ENIG (ELECTROLESS NICKEL / IMMERSION GOLD) 2-10 MICROINCHES OF GOLD OVER A MINIMUM OF
   120 MICROINCHES OF NICKEL PER IPC-4552. THIS FINISH COMPLIES WITH RoHS DIRECTIVES.
   ___ SELECTIVE HARD GOLD FINISH IN THE DUT AND POGOPAD AREA(S),
   CLASS 1 50-100 MICROINCHES THICK (KNOOP HARDNESS 130-200) OVER NICKEL PLATE IN
   ACCORDANCE WITH IPC-A-600, LATEST REVISION, SECTION 4.0, CLASS 3 (200-600 MICROINCHES THICK).
   FABRICATE IN ACCORDANCE WITH IPC-6018, GOLD OVERHANG CRITICAL, START WITH 1/4oz. COPPER
   ___ HASL (HOT AIR SOLDER LEVEL) SMT PADS MUST BE FLAT TO A MAX OF .003" ABOVE SURFACE. HASL FINISH
   TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH RoHS DIRECTIVES.
9. APPLY LPI (LIQUID PROTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840 CLASS T
   TO BOTH SIDES OF PCB. SOLDERMASK COLOR TO BE: _X_GREEN __BLUE __RED __CLEAR __BLACK __ORANGE.
   GERBER FILES REFLECT A ZERO OVERSIZE. FABRICATION VENDOR MAY OVERSIZE AS NEEDED, MAX THICKNESS .025mm (.001").
   IT IS ACCEPTABLE FOR SOLDERMASK WEBBING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.
10. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL SOLDER PADS.
    _X_TOP SIDE ONLY __BOTTOM SIDE ONLY __BOTH SIDES
11. FABRICATION VENDOR MAY REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS. FABRICATION VENDOR MAY
    ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.
12. TOLERANCES: WARP AND TWIST NOT TO EXCEED .010 IN/IN, CONDUCTOR WIDTHS/SPACINGS TO BE WITHIN +/-20%
    OF GERBER DATA. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381mm (.015") MAXIMUM. INSIDE CORNER MAXIMUM RADIUS
    _X_ NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.
    ___ MATRIX DRAWING PROVIDED, SEE FABRICATION DRAWING SHEET 2 OF 2.
    ___ VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY PEREGRINE
    SEMICONDUCTOR. PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK
    AWAY TABS. SEE DETAIL B. SUPPORT RAIL WIDTH TO BE 6.35mm (.25") - 12.7mm (.50") WITH
    1.52mm (.060") FIDUCIALS AND 3.175mm (.125") TOOLING HOLES IN 3 CORNERS
    PANELIZED SOLDERPASTE GERBER TO BE SUBMITTED TO PEREGRINE SEMICONDUCTOR.
13. PLANARITY:
    ___ VARIATION OF BUMP PADS IN THE Z AXIS TO BE <=5um.
    _X_ ALL 0.2032mm (.0079") VIAS TO BE EPOXY FILLED AFTER PLATING, PLANARIZED AND COPPER OVERPLATED
    AND BEFORE FINAL SURFACE FINISH. NON-CONDUCTIVE EPOXY (SAN_EI 900 OR EQUIVALENT) IS RECOMMENDED.
    EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES.
    A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.
    ___ ALL OTHER VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.
14. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST.
15. CONTROLLED IMPEDANCE REQUIREMENTS: FABRICATION VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT
    WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM PEREGRINE SEMICONDUCTOR.
    ___ NO CONTROLLED IMPEDANCE MEASUREMENTS REQUIRED.
    _X_ VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.
    ~~.XXmm (.XXX") TRACES ON LAYER Y ARE 50 OHMS, CO-PLANAR TRANSMISSION LINE ___+/-5% ___ +/- 10%.~~
    .2032mm (0.0079") TRACES ON LAYER 1 ARE 50 OHMS, MICROSTRIP, +/- 10%.
    ~~.XXmm (.XXX") TRACES ON LAYER Y ARE 100 OHMS, DIFFERENTIAL, +/- 10%.~~
16. SHORTS DESIGNED IN BOARD: ___ NO _X_ YES
    NET GND SHORTED TO NET RETURN, ON LAYERS 1, 2, 3 AND 4 AT C10 AND C22 COMPONENT LOCATIONS.

NOTE: DEVIATIONS BY FABRICATION FACILITY TO BE REPORTED TO PEREGRINE SEMICONDUCTOR.

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX= ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN D. KENDRICK	09-11-17
CHECKED GREG HORVATH	09-11-17
ISSUED	

COMPANY Peregrine Semiconductor
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TITLE
PCB, PE29102 CLASS D EVK

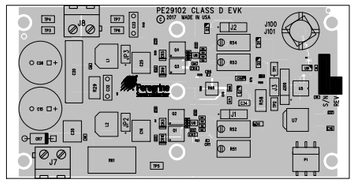
SIZE	RoHS COMPLIANCE RELEASE DATE	DWG NO.	REV.
C	Pb	PRT-69377	02

SCALE: NONE SHEET 1 OF 1

DWG NO.	SH	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



PRIMARY (TOP) SIDE

NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M.
2. WORKMANSHIP PER IPC-A-610D, CLASS 2.
3. COMPONENT LEAD PROTRUSION AND COMPONENT TO PCB GAP PER IPC-A-610D.
4. NO PARTS CONTAINING LEAD MAY BE INSTALLED ON THE ASSEMBLY WITHOUT THE PRIOR WRITTEN CONSENT OF PEREGRINE SEMICONDUCTOR.
5. ALL SOLDERING AND CLEANING PROCESSES FOR THIS ASSEMBLY MUST BE LEAD-FREE.
6. MANUAL ASSEMBLY AND REWORK MUST USE LEAD-FREE SOLDER AND FOLLOW RoHS PROCEDURES.
7. THIS ASSEMBLY IS RoHS COMPLIANT.
8. MANUFACTURER TO MARK ASSEMBLY WITH CURRENT REVISION LETTER.
9. FINISHED ASSEMBLY MUST BE FREE OF ANY RESIDUES.
10. PARTS USED ON THIS ASSEMBLY ARE TO HAVE DATE CODES WITHIN 24 MONTHS OF PURCHASE ORDER ISSUANCE DATE.
11. MANUFACTURE TO APPLY BARCODE LABEL IN SPACE PROVIDED.

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX= ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN D. KENDRICK	09-11-17
CHECKED GREG HORVATH	09-11-17
ISSUED	

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TITLE
ASY, PE29102 CLASS D EVK

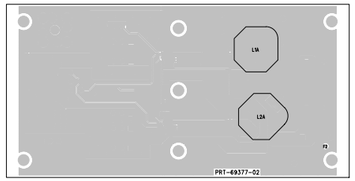
SIZE	RoHS COMPLIANCE RELEASE DATE	DWG NO.	REV.
C	Pb	PRT-69376	02

SCALE: NONE SHEET 1 OF 2

	DWG NO.	SH	REV

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



SECONDARY (BOTTOM) SIDE

SIZE	RoHS COMPLIANCE RELEASE DATE	DWG NO.	REV.
C	Pb	PRT-69376	02
SCALE: NONE		SHEET	2 OF 2