High Power Handling in UltraCMOS® Devices

What is Maximum Linear Power?

The further a signal needs to travel the greater the required power. As the power increases so does the magnitude of the unwanted spurious signals. These spurious affect other systems; these can be complex communication scenarios where different systems can be located in frequency bands very close to each other, such as a simple garage door opener and cellular phone in close proximity. The spurious emissions are defined by the linearity of the device, so it is critical that the device can handle high power while simultaneously maintaining high linearity.

Many of the high power applications are becoming more complex as end products need to support multiple frequency bands or signal paths. This added complexity means a small footprint is essential in order to fit the additional features into an acceptable volumetric size.

Peregrine defines its high power capability as the maximum input power that the device can handle without degrading the linearity of the product. In this definition the maximum input power level is not directly related to the 1dB compression point (P1dB), which is different from products designed on more traditional high power processes such as Gallium Arsenide (GaAs). Customers that are used to GaAs products expect to see linearity degradation occur at the P1dB and will specify the input power with margin to the P1dB in order to guarantee no reduction in the linearity performance.

For an UltraCMOS® product, no additional margin is required because the maximum input power occurs before the 1dB compression point and this means there is no linearity degradation at the maximum input. This concept is illustrated in Figure 1 which shows the performance of the PE42580 SP5T 42 dBm (CW) switch, the graph shows that the output power is not compressing but the harmonics start to increase at approximately 45.6 dBm of CW input power.

Figure 1. Measured data on PE42850: Input Power vs. Output Power and 2nd & 3rd Harmonic Performance
Benefits of UltraCMOS

The UltraCMOS process uses a high resistivity substrate that minimizes substrate losses and parasitic capacitances. This reduces insertion loss and dissipated power, which simplifies thermal management of the device. High power handling is realized with low voltage FET’s by using a stacking technique to create a “virtual high voltage CMOS FET” which is possible due to the high isolation of UltraCMOS. The high isolation is important in order for the voltage across the FET (VDS) to be equally distributed. The concept is illustrated in Figure 2.

HaRP™ is a design technique that significantly improves the linearity of the FET across the designed operating range (frequency, power, supply voltage and temperature), when combined with the UltraCMOS technology it uniquely enables Peregrines products to be highly linear up to the maximum operating power the device is specified to operate at. This capability means that the products can be optimized for low insertion loss, isolation, and size. This enables improved system performance, long battery life and low total cost.

High Power RF Switches

UltraCMOS® technology delivers unprecedented combination of 30W power handling and excellent linearity across the UHF/VHF through LTE frequency bands.

The PE42820 and PE42821 are ideal for transmit/receive, filter bank and antenna band switching applications in high-power RF systems such as wireless infrastructure devices and land-mobile-radio (LMR) for public safety and military environments.

The PE42850 and PE42851 high power, high linearity switches utilize UltraCMOS and HaRP technologies. They are configurable as either SP3T or SP5T switches and support 42 dBm (17W) continuous wave or 45 dBm (32W) pulsed wave with harmonic performance as low as −90 dBC @ 1.15:1 VSWR

- Exceptional power handling: 17 Watt CW
- Broad bandwidth: 30 MHz up to 2.7 GHz
- High linearity: $2f_o/3f_o$ as low as −90 dBC @ 1.15:1 VSWR
- Low power consumption of 130 µA @ 3.4 V