8-Channel Beamforming Front End and *Dual-Channel Up-Down Converter* in 5G FR2 RF Front End (RFFE)

PE188100: *n258 (26 GHz) 8-channel Beamforming Front End*
PE188200: *n257 (28 GHz) 8-channel Beamforming Front End*
PE128300: *n258/n257/n261 (26/28 GHz) Dual-Channel Up-Down Converter*

Applications Engineering
pSemi, a Murata company

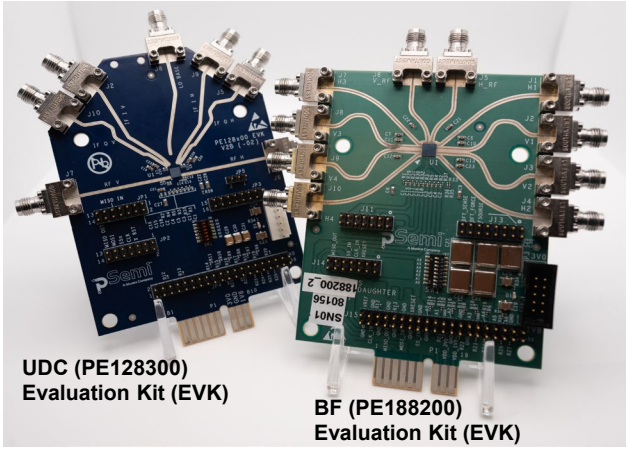
Presentation Overview

- 5G FR2 RF Front End (RFFE) Architecture
- Antenna Array and Beams
- 8-Channel Beamformer (PE188X00)
- Wideband Dual-Channel Up-Down Converter (PE128300)
- Evaluation Kit and Software

5G FR2 RF Front End (RFFE)

Typical 5G FR2 RF Front End (RFFE)

- A typical RFFE is composed of:
  - Antenna array
  - Beamformer (BF)
  - Up-Down converter (UDC)
- pSemi produces BF and UDC ICs for 5G NR FR2 RFFE
  - The 8-channel BF (PE188X00) controls the beam direction and shape.
  - The wideband dual-channel UDC (PE128300) converts
    - The received RF signals down to the IF band and
    - The modulated IF signals up to the RF band.



Part #	Description	5G NR band	Min Freq	Max Freq
PE188100	n258 8-Channel Beamformer (BF)	n258 (26 GHz)	24.25 GHz	27.5 GHz
PE188200	n257 8-Channel Beamformer (BF)	n257 (28 GHz)	26.5 GHz	29.5 GHz
PE128300	WB Dual-Channel Up-Down Converter (UDC)	n258/257/261 (26/28 GHz)	24.25 GHz	29.5 GHz

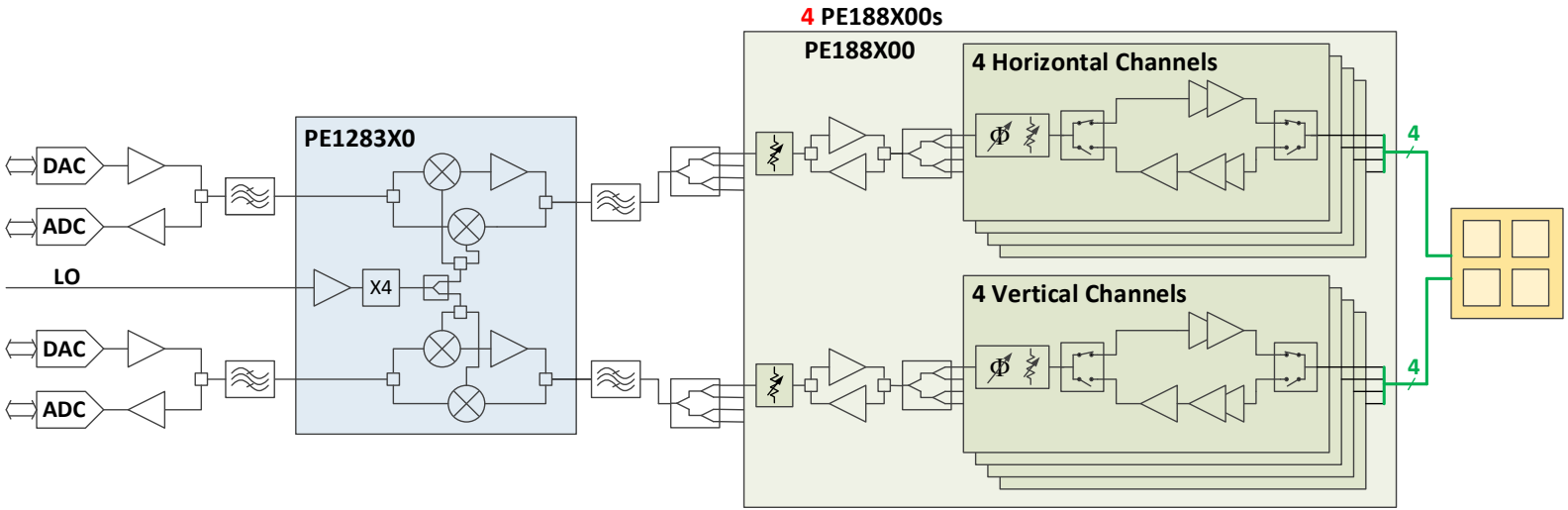
Product Information

	PE188100 8-Channel BF	PE188200 8-Channel BF	PE128300 WB Dual-Channel UDC
5G Band	n258	n257	n258 / n257 / n261
Frequency Range	24.25 GHz – 27.5 GHz	26.5 GHz – 29.5 GHz	24.25 GHz – 29.5 GHz
Package	3.55 x 3.63 mm flip-chip die		4.35 x 4.35 mm Flip chip die
Features	• Compatible with PE1283X0 • Fast beam switching • Integrated PAs and LNAs • Optimized for dual-polarity antenna arrays* • 8 channels with independent phase/attenuation controls - 7-bit attenuation control - 8-bit phase control • On-chip memory for 512 beam control settings • Liner Pout = + 9.5 dBm (CP-OFDM 64QAM)		• Compatible with PE188X00 • Fast TDD switching (< 400ns) • Optimized for dual-polarity antenna arrays* • Common LO x4 multiplier • Image rejection with I/Q balance adjustments • Multiplied LO phase adjustments • IF phase/gain adjustments • TX OP1dB = +14 dBm • RX IIP3 = +7 dBm • RX NF = 6.0 dB

*Application can extend to other antenna configurations

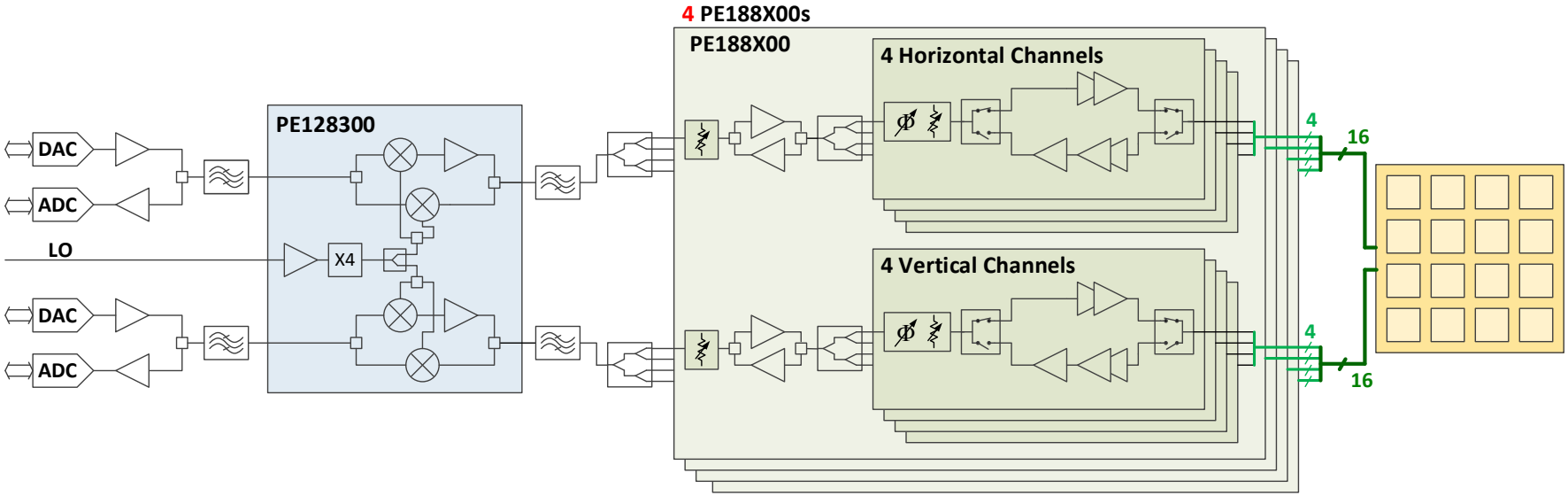
Typical 5G FR2 RFFE with pSemi ICs

- 2 x 2 (4) Dual-polarity Antenna Array



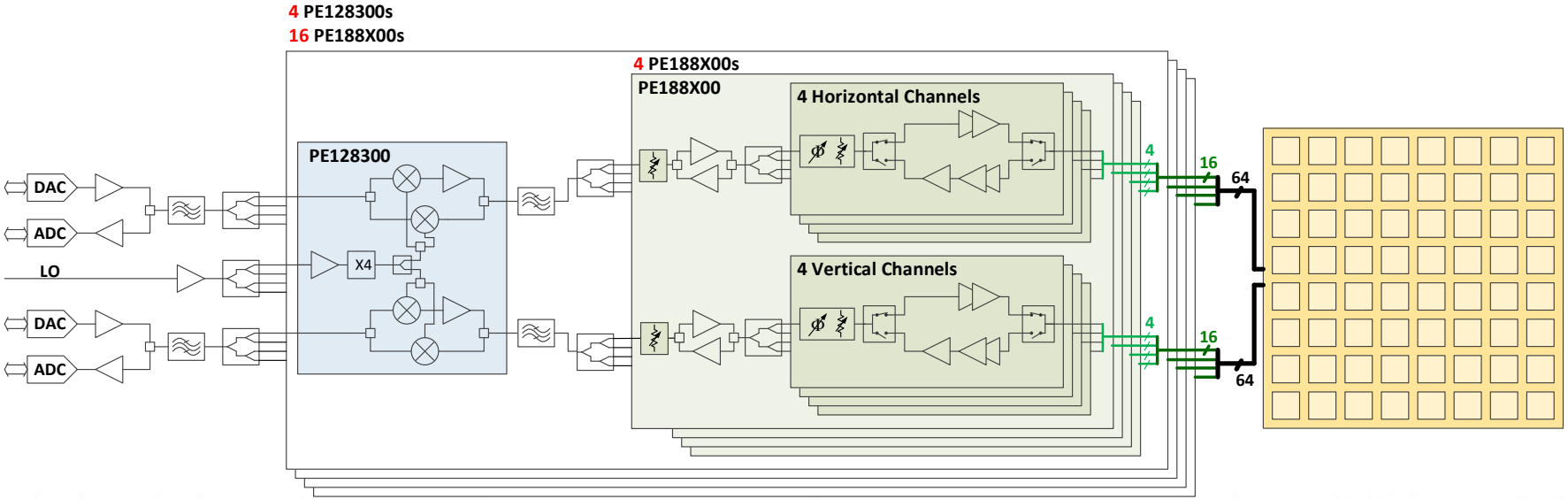
Typical 5G FR2 RFFE with pSemi ICs

- 4 x 4 (16) Dual-polarity Antenna Array

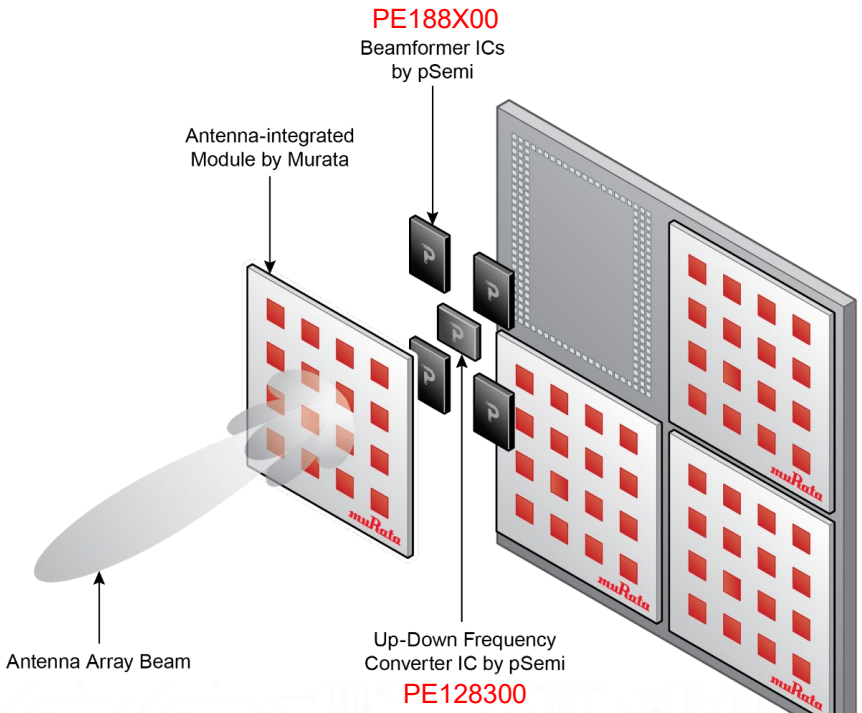


Typical 5G FR2 RFFE with pSemi ICs

- 8 x 8 (64) Dual-polarity Antenna Array



Summary of 5G FR2 RFFE with pSemi ICs



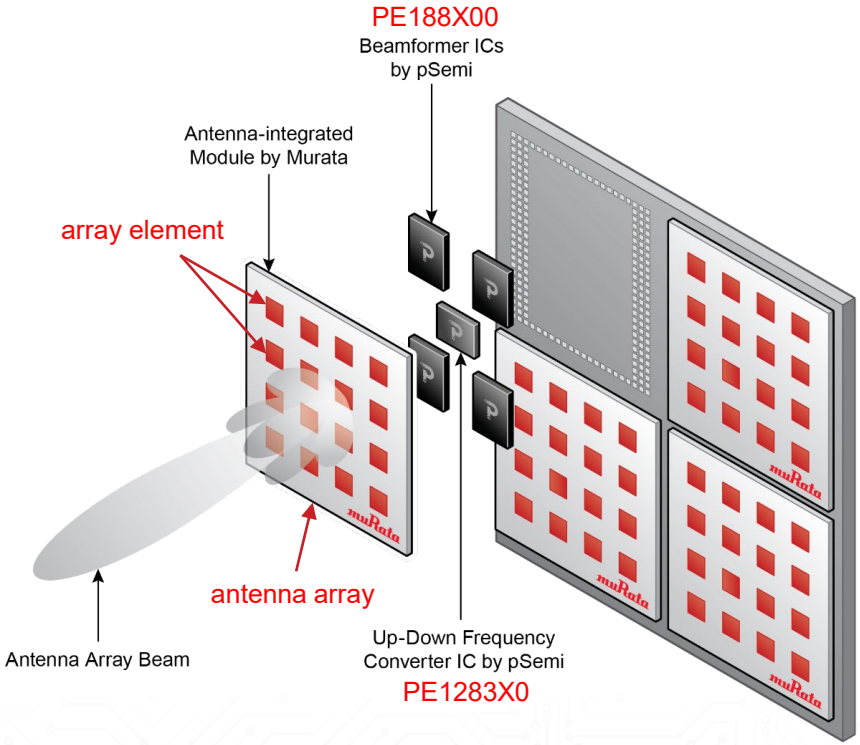
N x N Dual-polarity Antenna Configuration	# of PE128300s Required	# of PE188X00s Required
4 (2 x 2)	1	1
16 (4 x 4)	1	4
64 (8 x 8)	4	16
256 (16 x 16)	16	64

- Antenna-integrated modules are available from Murata.
- UDC (PE128300) and BF (PE188X00) are optimized for dual-polarity antennas.
- UDC (PE128300) and BF (PE188X00) apply to antenna types/configurations.

Antenna Array & Beams

Antenna Array

- Antenna arrays are composed of array elements.
- The polarization of array elements can be either *single* or *dual.*
  - *Single-polarity*: Transmits/receives EM waves in a plane (2D space).
  - *Dual-polarity*: Transmits/receives EM waves in a 3D space.
- “Beam” illustrates a path of transmit and receive in a 3D space.
- In a typical RFFE system, the beamformer IC (i.e., PE188X00) controls the direction and shape of the beam.



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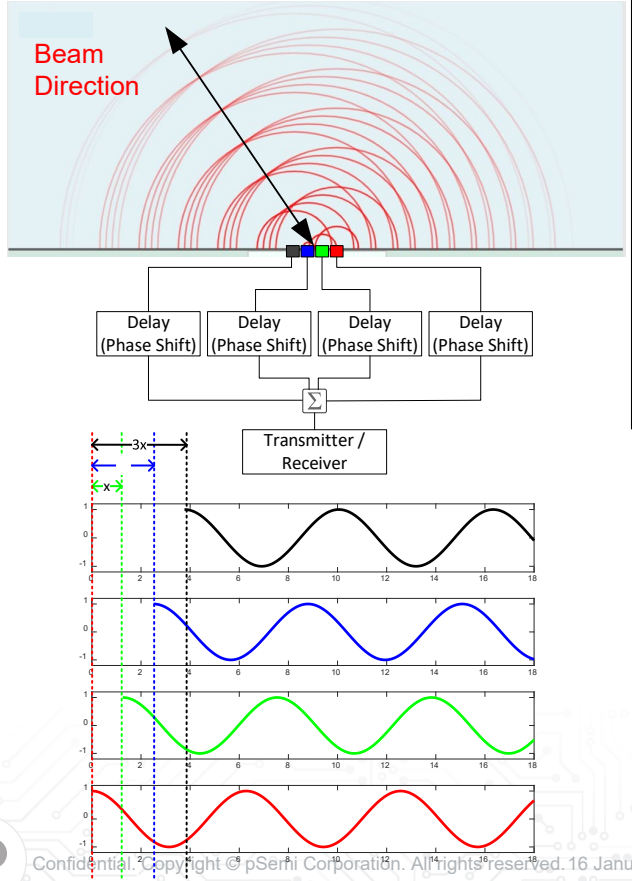
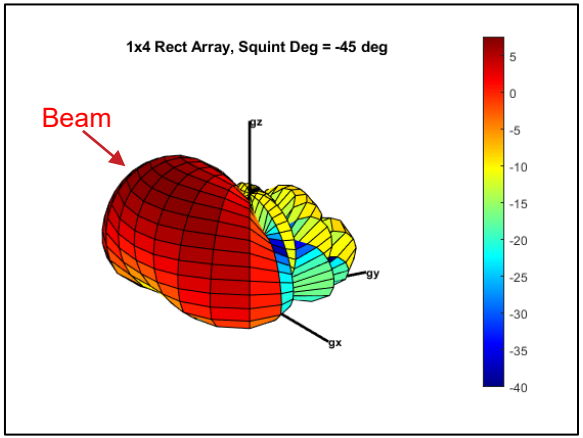
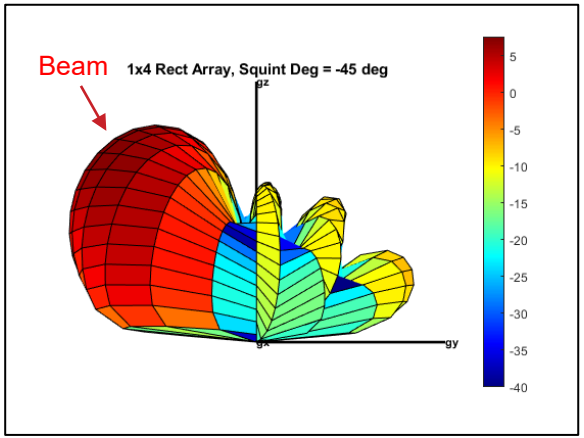
Beams of Linear Antenna Array (Single-Polarity)







- 4 x 1 linear phased array is illustrated without amplitude adjustments.
- Transmits/receives EM waves in the y-z plane.
- The time delays (phase shift) to each antenna element are carefully adjusted to create a beam at -45° from the z-axis.
  - 1st element's time delay = 3*x sec
  - 2nd element's time delay = 2*x sec
  - 3rd element's time delay = 1*x sec
  - 4th element's time delay = 0 sec (reference)

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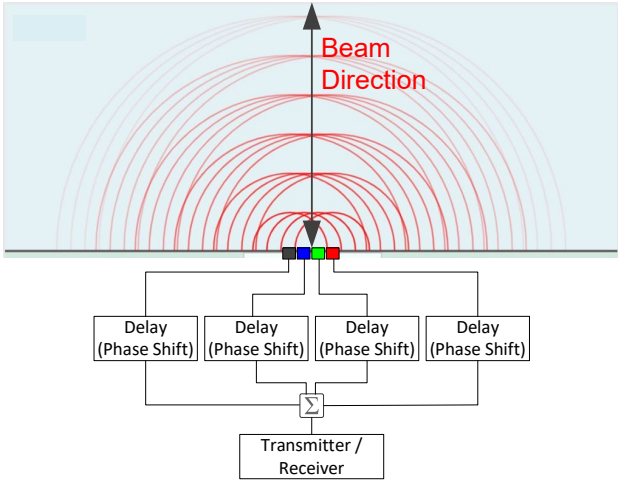
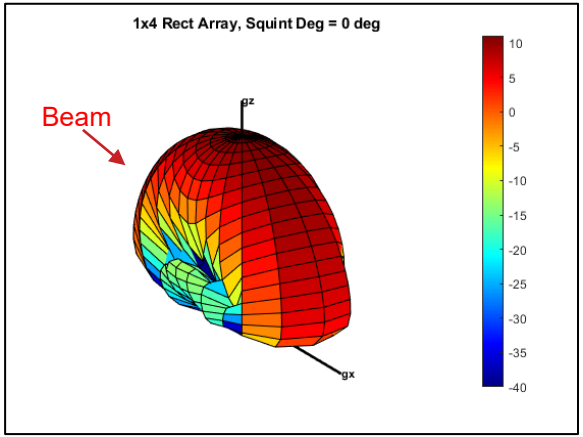
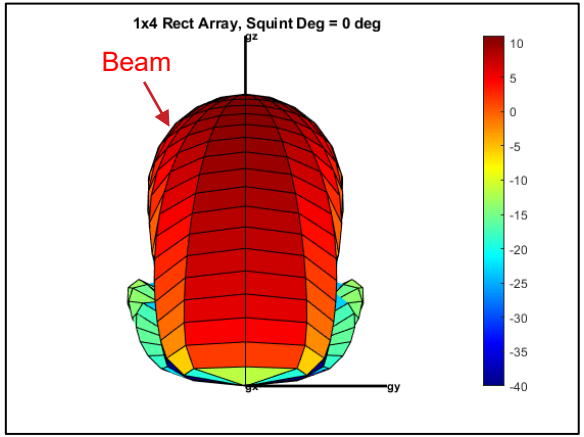
Beams of Linear Antenna Array (Single-Polarity)







- 4 x 1 linear phased array is illustrated without amplitude adjustments.
- Transmits/receives EM waves in the y-z plane.
- The time delays (phase shift) to each antenna element are equalized to create a beam at 0° from the z-axis.
  - 1st element's time delay = 0 sec
  - 2nd element's time delay = 0 sec
  - 3rd element's time delay = 0 sec
  - 4th element's time delay = 0 sec

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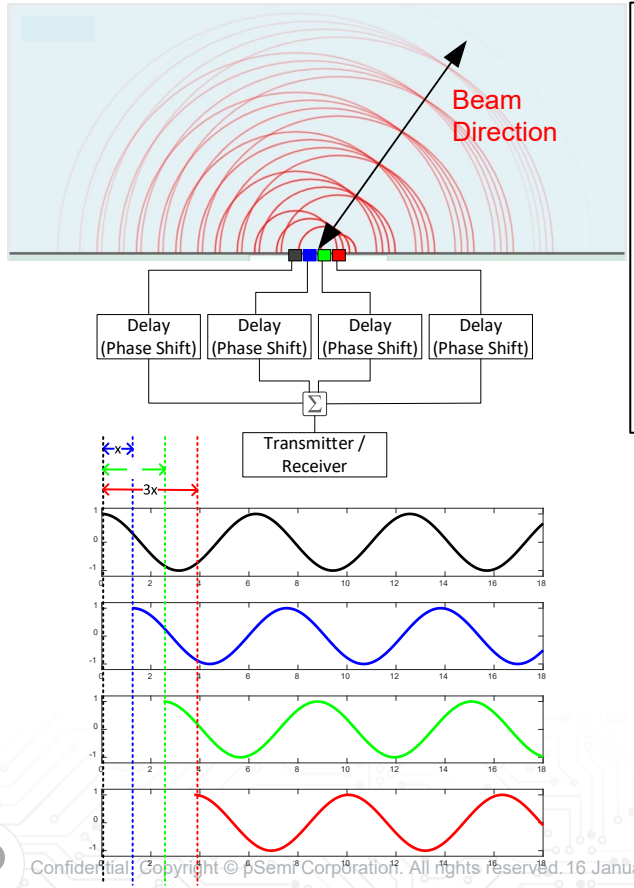
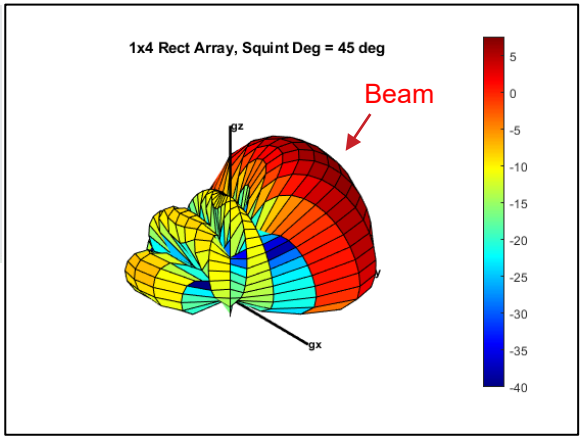
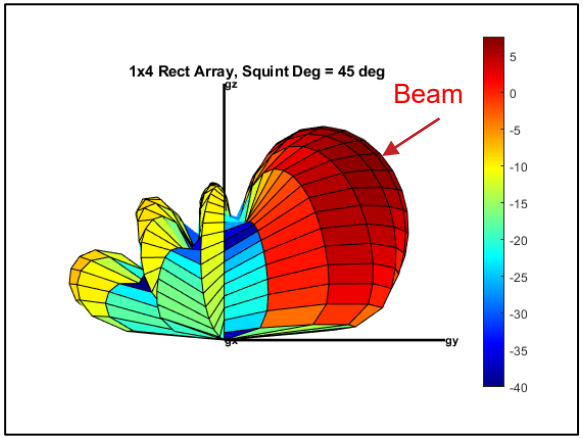
Beams of Linear Antenna Array (Single-Polarity)

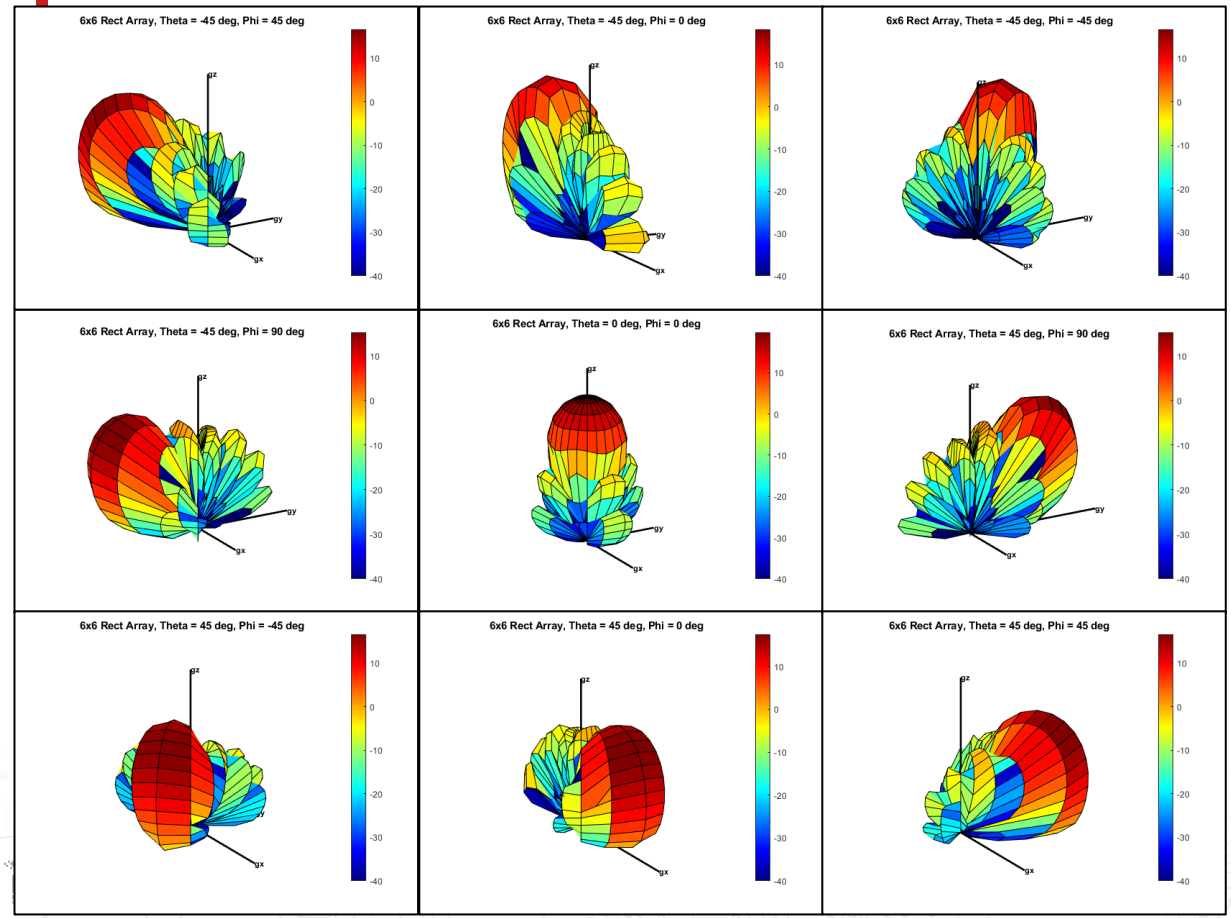






- 4 x 1 linear phased array is illustrated without amplitude adjustments.
- Transmits/receives EM waves in the y-z plane.
- The time delays (phase shift) to each antenna element are carefully adjusted to create a beam at +45° from the z-axis.
  - 1st element's time delay = 0 sec (reference)
  - 2nd element's time delay = 1*x sec
  - 3rd element's time delay = 2*x sec
  - 4th element's time delay = 3*x sec

Example: Beams of 4 x 4 Antenna Array (Dual-Polarity)

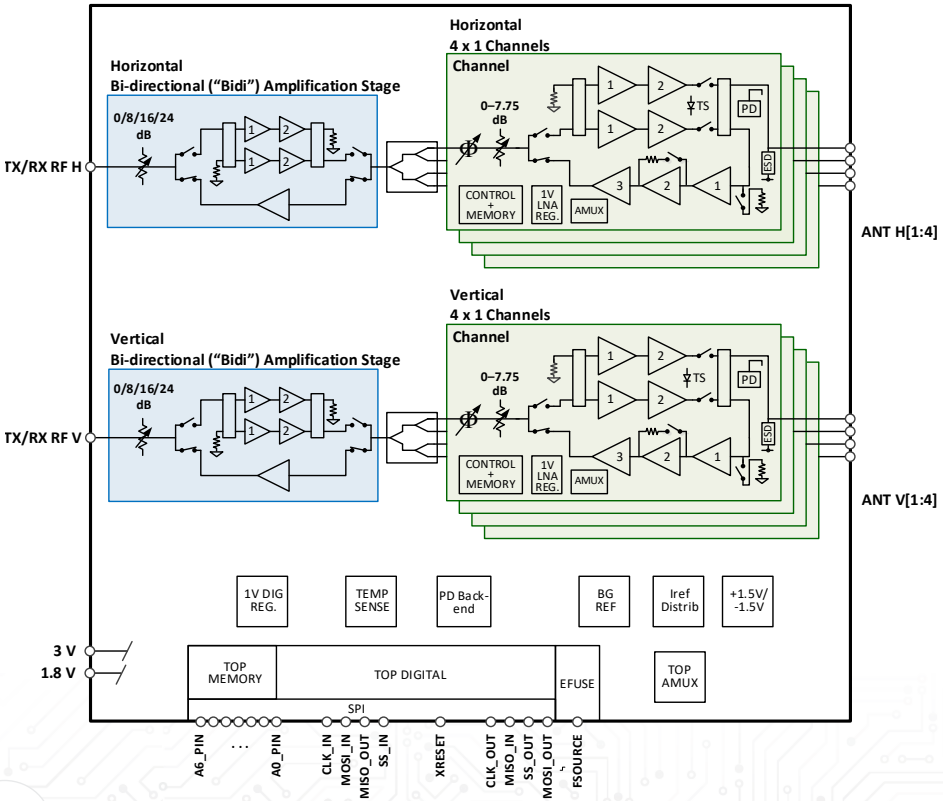


- 4 x 4 antenna array is illustrated
- The time delays can be adjusted in horizontal and vertical directions.
- Allows beam to point anywhere in a 3D space (x-y-z axes).
- The PE188X00 is optimized for an N x N dual-polarity antenna array.
- The PE188X00 controls the phase and amplitude of each antenna element to form a beam in a desired direction as illustrated.

N x N Dual-polarity Antenna Configuration	# of PE128300s Required	# of PE188X00s Required
4 (2 x 2)	1	1
16 (4 x 4)	1	4
64 (8 x 8)	4	16

8-Channel Beamformer
PE188X00

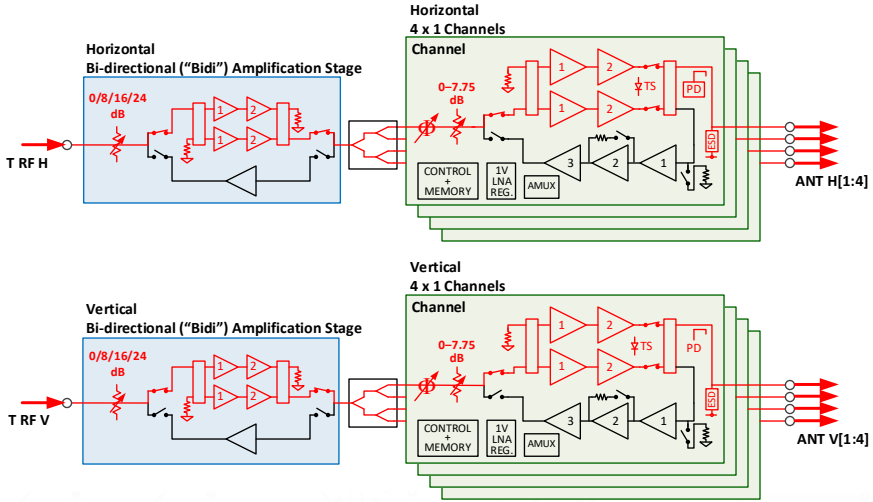
PE188X00 Overview



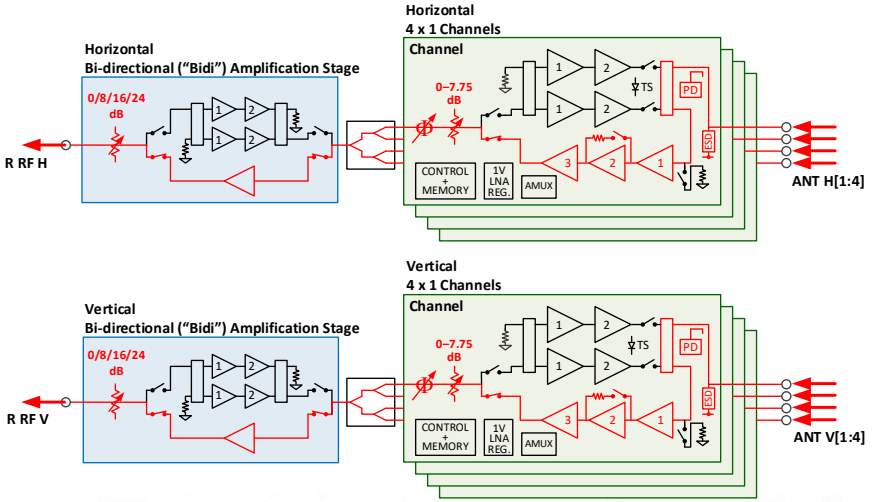
- The PE188X00 is an 8-channel beamforming front end for 5G millimeter wave applications.
- The PE188X00 has two independent RF paths of four channels (4 horizontal and 4 vertical) to support dual-polarity antennas.
- The utilization of on-chip memory (LUT and registers) is essential in operating the PE188X00.
- The serial parallel interface (SPI) is used for:
  - Writing to the on-chip memory (initialization)
  - Reading from the on-chip memory (initialization)
  - Selecting the device modes (operation)
  - Selecting the beam formation (operation)

PE188X00 Overview – RF Signal Flow for TX and RX

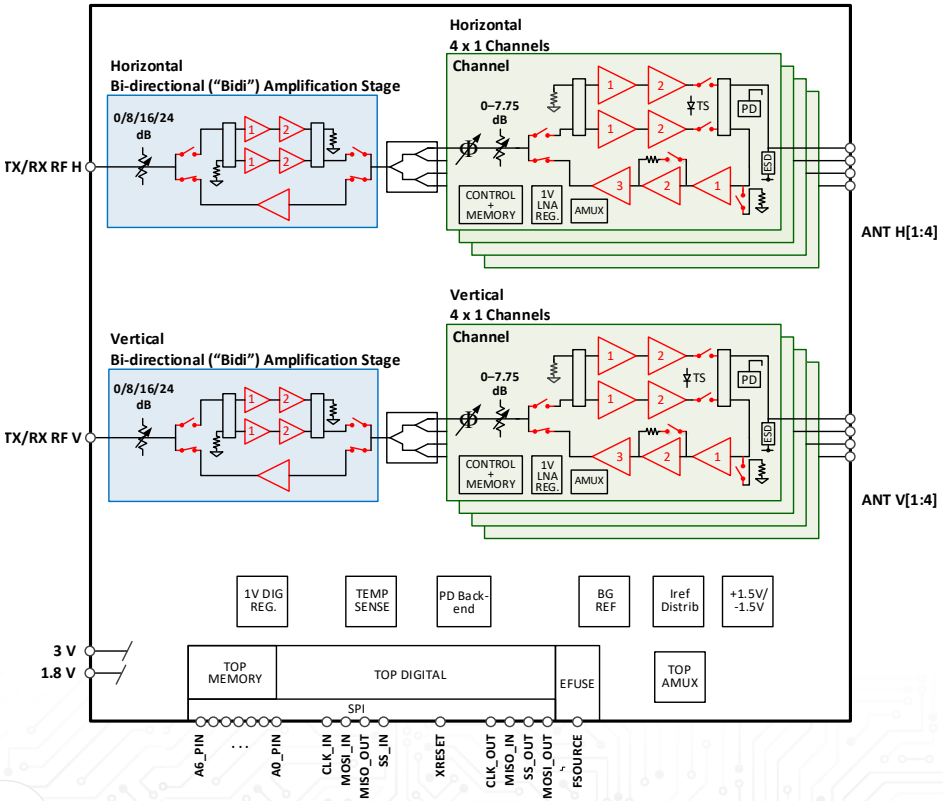
TX Signal Flow (*All TX* mode)



RX Signal Flow (*All RX* mode)

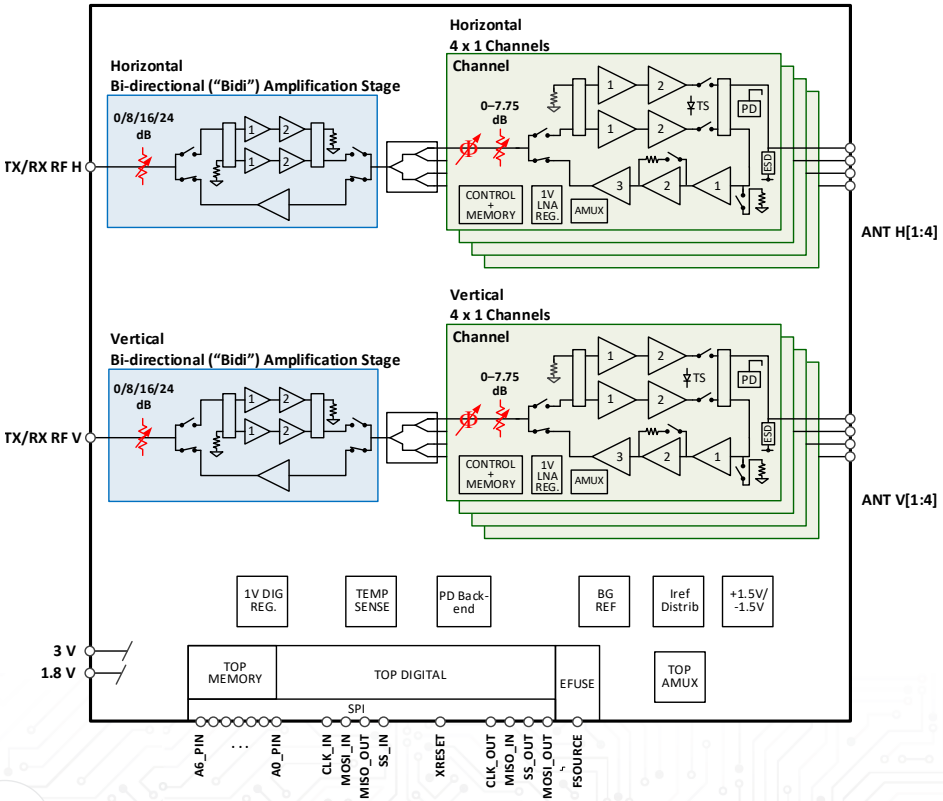


PE188X00 Overview – Modes vs. Amplifier/SPST Settings



- The PE188X00 supports up to 32 modes. (Only 11 modes are defined in the default configuration.)
- The default modes are:
  - All neutral
  - All TX
  - All RX
  - Only H TX
  - Only V TX
  - Fast neutral
  - Loopback (V to H)
  - Loopback (H to V)
  - All RX w/ -6 dB attn
  - H RX w/ -6 dB
  - V RX w/-6 dB
- Each mode requires a unique combination of control settings for:
  - SPST switches
  - Amplifier enables
  - Amplifier bias levels

PE188X00 Overview – Beams vs. DSA/DPS Settings



- The PE188X00 stores up to 512 beam settings.
- The PE188X00 is optimized for 4 dual-polarity antenna elements
  - Eight bi-directional channels (4 horizontal and 4 vertical) with independent amplitude and phase controls:
    - 5-bit DSA (0 – 7.75 dB) per channel
    - 8-bit DPS per channel
  - Two common amplification stages for combined horizontal/vertical channels.
    - 2-bit DSA (0/8/16/24 dB) per stage
- Each beam requires a unique combination of control signals for the DSAs and DPSs.

Theory of Operation

- Impractical to send control bits over the serial interface at every mode/beam change.
  - +700 control bits for a given mode
    - SPST switches
    - Amplifier enables
    - Amplifier bias levels
  - +800 control bits for a given beam
    - DPS/DSA settings

- The PE188X00 utilizes lookup tables (LUTs) on on-chip memory to store control bits.
  - 32 stories for modes
  - 512 stories for beams

- The mode/beam is changed by indexing the LUT via the SPI.
  - 5 bits to “lookup” modes
    - Sends out one of the 32 sets of control bits (from the LUTs) to amplifiers/SPSTs.
  - 9 bits to “lookup” beams
    - Sends out one of the 512 sets of control bits (from the LUTs) to DSAs/DPSs.

Initialization

- The on-chip memory (volatile), which contains 6 LUTs and 2 registers, must be “initialized” at each power-up or reset.
  - LUTs: *DPS LUT*, *DSA LUT*, *Channel-mode LUT*, *Bias-mode LUT*, *H Top-mode LUT*, *V Top-mode LUT*
  - Registers: *Channel Static RF/Analog Control Registers*, *Top Static RF/Analog Control Registers*

- *Initialization* means loading the LUTs and registers with the “right” contents (control bits).
  - Contents (control bits) are application-specific.
  - Contents (control bits) are either provided by pSemi or defined by the user.
  - Serial parallel interface (SPI) is used to load.

- The contents (control bits) are transferred and written to LUTs and registers during initializations.
  - *Bias-mode LUT* – transferred from eFuse*
  - All other LUTs and registers – written (values are either provided or defined)

- eFuse
  - Non-volatile memory on PE188X00.
  - Contents are burned during production.
  - Stores calibration and manufacturing information.

Initialization Contents and Recommendations

- Bias-mode LUT
  - Contents are transferred from eFuse.
- DPS LUT, DSA LUT
  - Default contents are provided by pSemi.
  - Users must re-define the contents.
- H Top-mode LUT, V Top-mode LUT, Channel-mode LUT
  - Default contents are provided by pSemi (provides 11 frequently used modes).
  - Users must use the default contents.
- Channel Static RF/Analog Control Registers, Top Static RF/Analog Control Registers
  - Default contents are provided by pSemi.
  - Users must use the default contents.

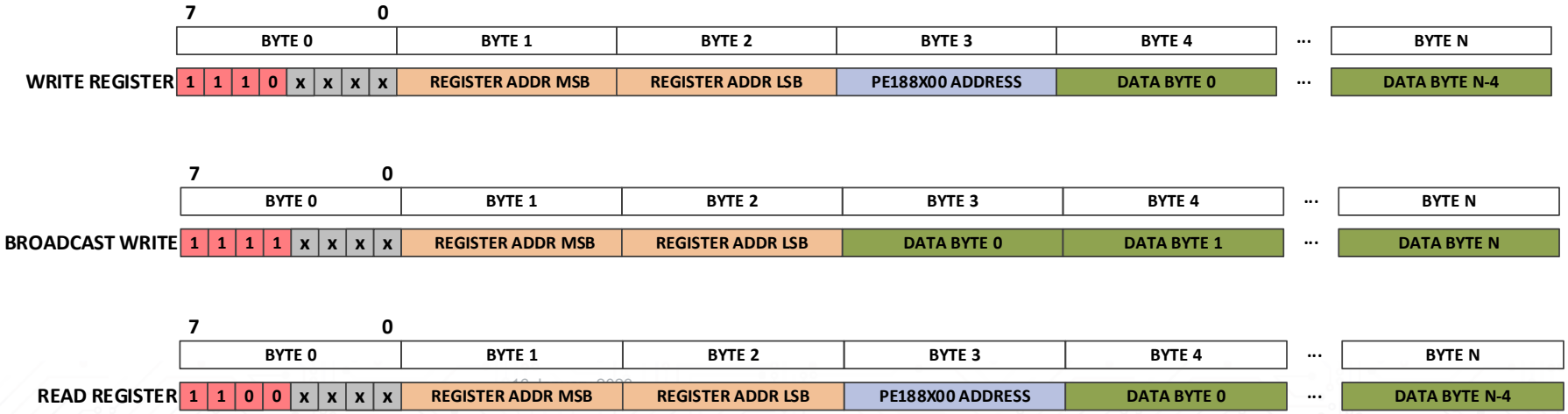
LUT / REGISTER NAME	LUT AND REGISTER CONTENTS AND DESCRIPTION	INITIALIZATION CONTENT	SIZE (BITS)
DPS LUT	512 discrete control settings for DPS (allows maximum of 512 unique beams)	Defined by user[1]	2^9 ×8
DSA LUT	512 discrete control settings for DSA (allows maximum of 512 unique beams)	Defined by user[1]	2^9×7
Channel-mode LUT	Enable bits and switch control bits for amplifiers in all channels	Provided by pSemi[2]	2^5 × 15
Bias-mode LUT	Control bits for amplifier bias currents for amplifiers in all channels	Transferred from eFuse	2^1 × 80
H Top-mode LUT	Enable bits and switch control bits for each amplifier in the bi-directional amplification stage for 4 horizontal channels.	Provided by pSemi	2^5 × 7
V Top-mode LUT	Enable bits and switch control bits for each amplifier in the bi-directional amplification stage for 4 vertical channels.	Provided by pSemi	2^5 × 7
Channel Static RF/Analog Control Registers	Enable bits and control bits for self-test, RF circuit configuration, power-up configuration, calibration, and miscellaneous functions.	Provided by pSemi	83 × 8
Top Static RF/Analog Control Registers	Enable bits and control bits for RF circuit configuration, power-up configuration, calibration, and miscellaneous functions.	Provided by pSemi	485
Top Static Digital Registers	Enable bits and control bits for self-test. Not relevant to users.	N/A	23

[1] Default contents provided by pSemi are optimized for 4×4 dual-polarity antenna arrays at the component level.

[2] Default contents provided by pSemi are recommended when integrating with PE1283X0.

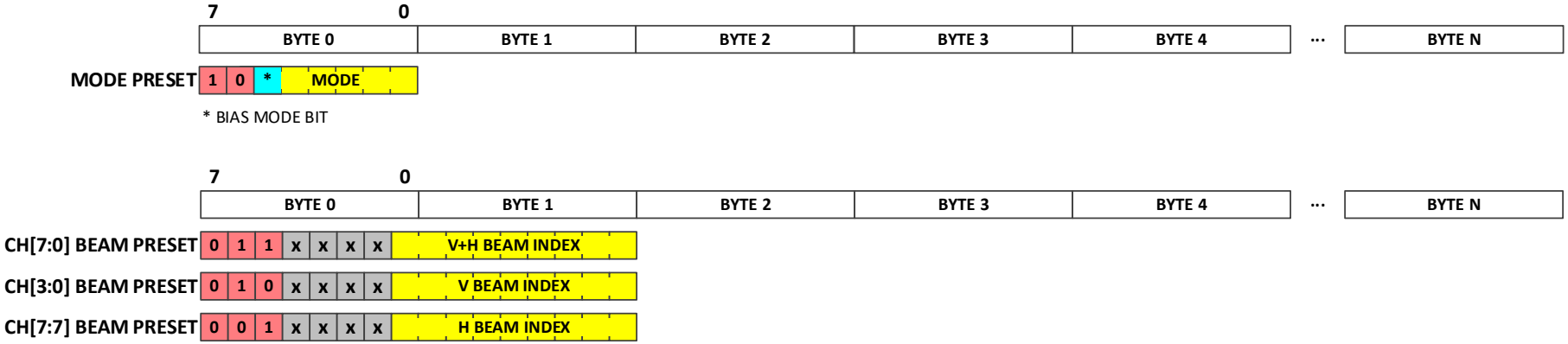
SPI Commands (Initialization) – Writing and Reading

- The details are covered in the PE188X00 User's Manual.
- The WRITE REGISTER and BROADCAST WRITE commands write/transfer contents to the LUTs and registers during initialization.
- The READ REGISTER command verifies the writes.



SPI Commands (Operation) – Selecting Mode and Beam

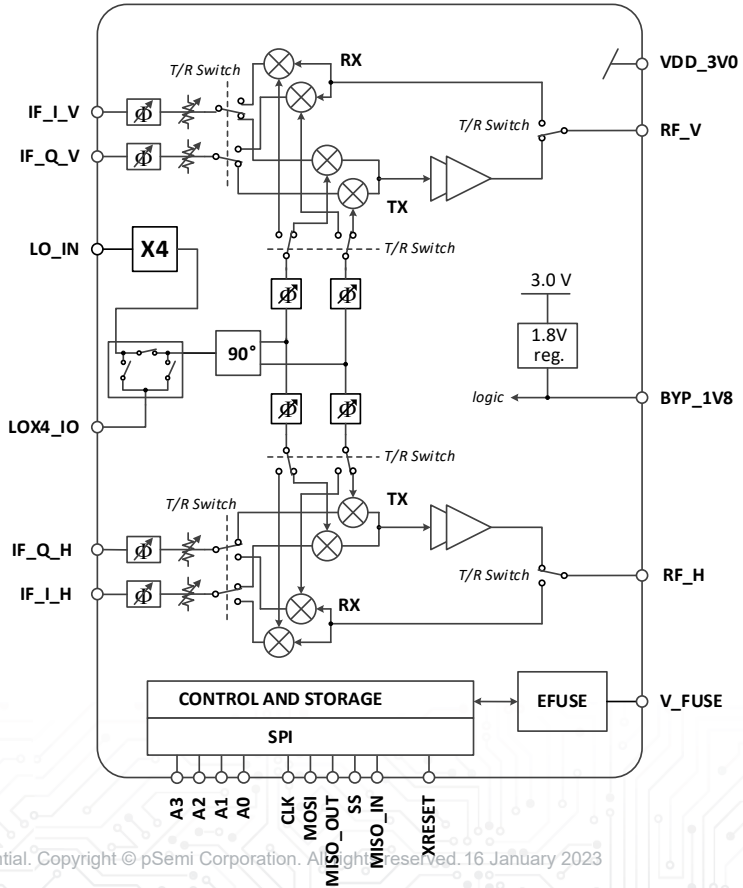
- The details are covered in the PE188X00 User's Manual.
- The MODE PRESET command selects one of the 32 pre-stored modes during operation.
- The BEAM PRESET command selects one of the 512 pre-stored beams during operation.



Wideband Dual-Channel Up-Down Converter

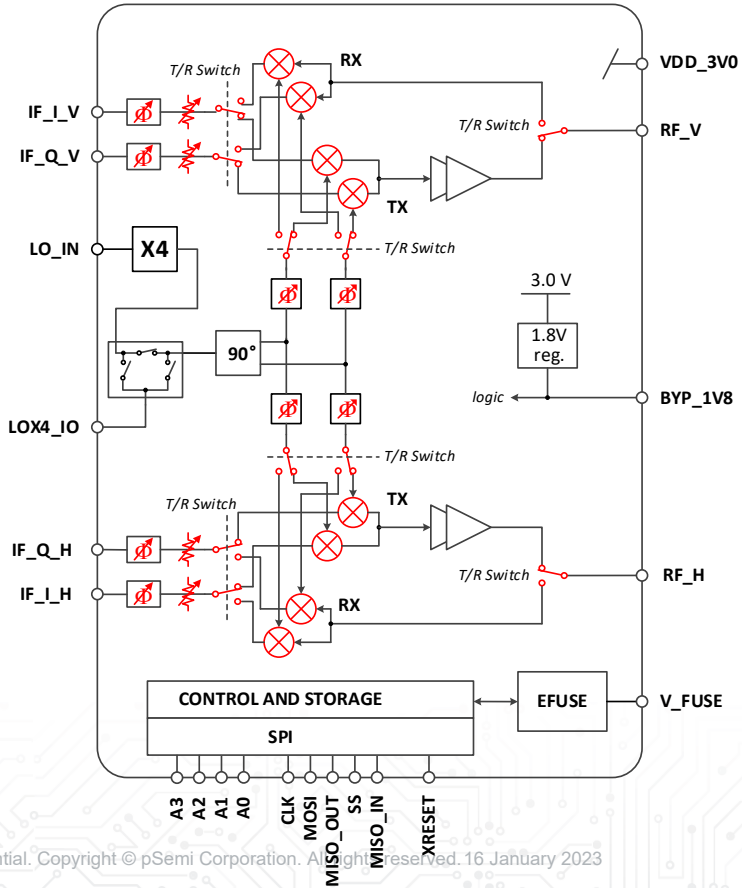
PE128300

PE128300 Overview



- The pSemi PE1283X0 is a dual-channel time division duplex (TDD) up-down converter designed for 5G millimeter wave applications.
- PE1283X0 is has two identical RF channels, the H channel and V channel, which are bi-directional.
- The utilization of on-chip memory (LUT and Registers) is essential in operating the PE188X00.
- The serial parallel interface (SPI) is used for:
  - Writing to the on-chip memory (initialization)
  - Reading from the on-chip memory (initialization)
  - Selecting the device modes (operation)

PE128300 Overview – Modes



- The PE128300 supports up to 32 modes (only 11 modes are defined in the default configuration).
- The default modes are:
  - All neutral
  - All TX
  - All RX
  - Only H TX
  - Only V TX
  - Fast neutral
  - Loopback (V to H)
  - Loopback (H to V)
  - All RX w/ -6 dB attn
  - H RX w/ -6 dB
  - V RX w/-6 dB
- Each mode requires a unique combination of control settings for:
  - T/R switches
  - DPS/DSA
  - Mixer enables

Theory of Operation and Initialization

Theory of Operation

- The lookup table (LUT) on on-chip memory stores 32 sets of control bits for T/R switches, DPSs, DSAs and mixers.
- The default contents (control bits) for the LUT provide 11 modes, which are compatible with the PE188X00.
- The mode is changed by indexing the LUT via the SPI
  - Sends out control bits (from the LUT) to T/R switches, DPSs, DSAs and mixers.

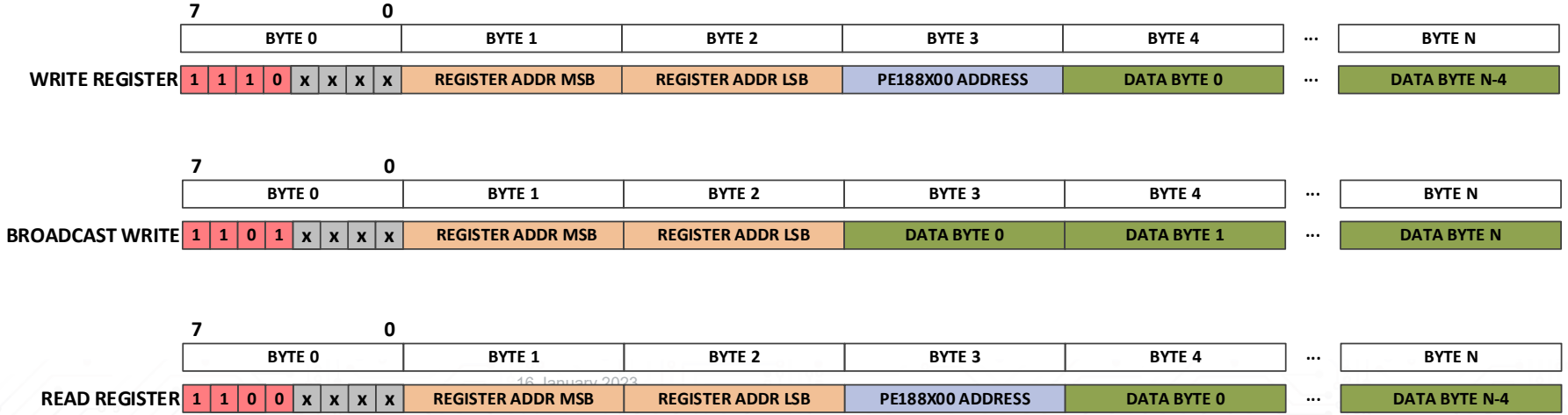
Initialization

- The on-chip memory (volatile) must be “initialized” at each power-up or reset.
- Static register
  - Contents are transferred from eFuse.
- Mode LUT and other registers
  - Contents are provided by pSemi.
  - Users must use the default contents.

LUT/REGISTER NAME	LUT AND REGISTER CONTENTS/DESCRIPTION	INITIALIZATION CONTENT
IF Gain/Phase Adjust Registers	Gain and phase control bits and switch control bits for IF I and Q signals	Provided by pSemi
LO Gain/Phase Adjust Registers	Gain and phase control bits and switch control bits for LO signal	Provided by pSemi
Mode LUT	32 discrete mode settings for PE1283X0	Provided by pSemi
Static Registers	Enable bits and control bits for power-up configuration, calibration, and miscellaneous functions.	Transferred from eFuse

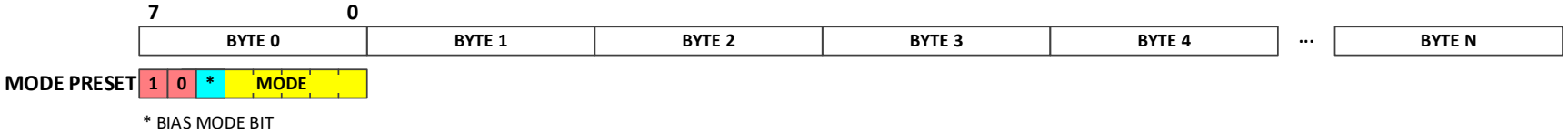
SPI Commands (Initialization) – Writing and Reading

- The details are covered in the PE1283X0 User's Manual.
- The WRITE REGISTER and BROADCAST WRITE commands write/transfer contents to the LUTs and registers during initialization.
- The READ REGISTER command verifies the writes.



SPI Commands (Operation) – Selecting Mode

- The details are covered in the PE188X00 User's Manual.
- The MODE PRESET command selects one of the 32 pre-stored modes during operation.

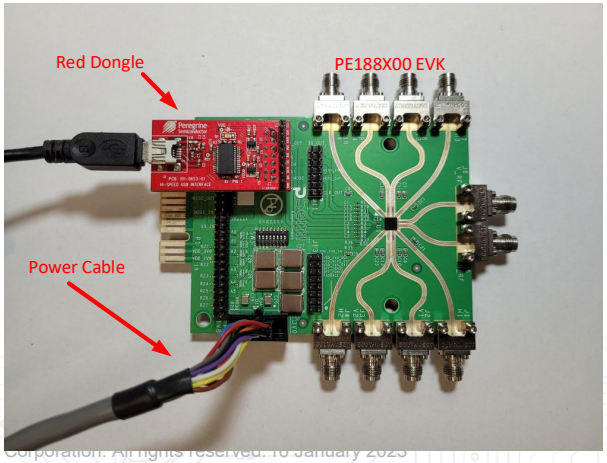


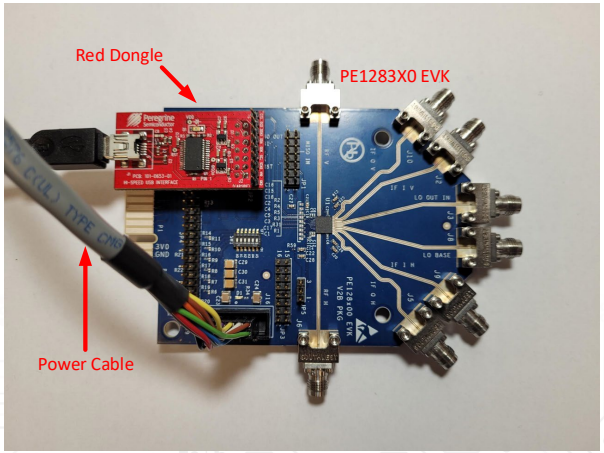
Evaluation Kit and Software

EVK and GUI Overview

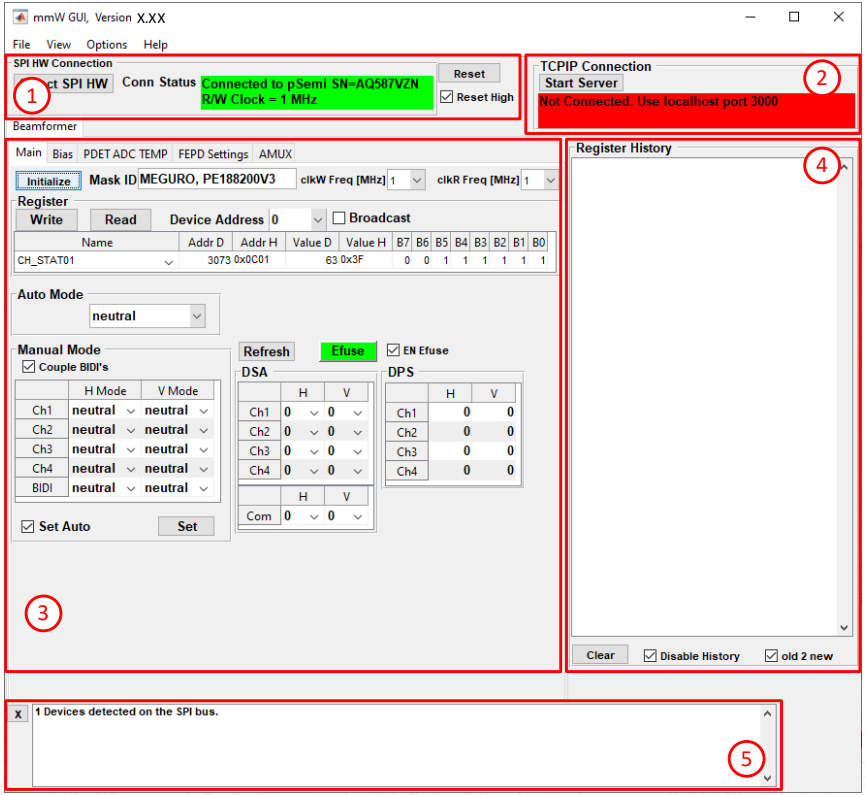
- *mmW GUI* – Evaluation Software for PE188X00
- *Mixer Control GUI* – Evaluation software for PE128300
- Red dongle is provided.

Part #	Description	5G NR band	Min Freq	Max Freq
PE188100	n258 8-Channel Beamformer (BF)	n258 (26 GHz)	24.25 GHz	27.5 GHz
PE188200	n257 8-Channel Beamformer (BF)	n257 (28 GHz)	26.5 GHz	29.5 GHz
PE128300	WB Dual-Channel Up-Down Converter (UDC)	n258/257/261 (26/28 GHz)	24.25 GHz	29.5 GHz





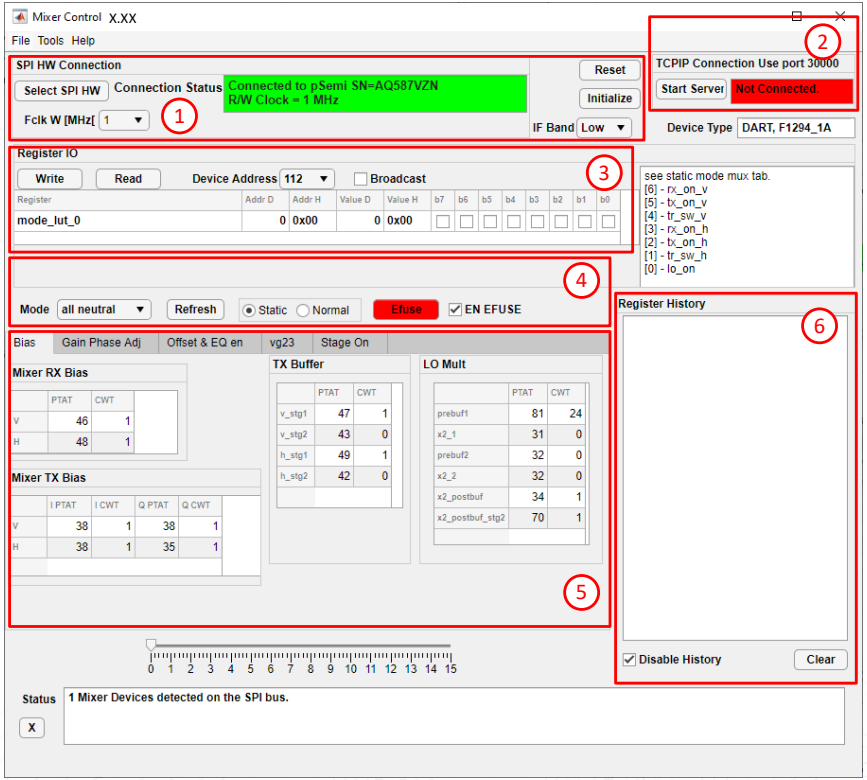
mmW GUI – Evaluation Software for PE188X00



mmW GUI Main	Figure Ref.	Description
SPI HW Connection	①	Connects to SPI master device, displays SPI connection status, and resets SPI connection.
TCPIP Connection	②	Allows custom MATLAB scripts to utilize the tools in mmW GUI for automation, calibration, etc.
Beamformer Control	③	Controls beamformer; it includes 5 functional tabs: **Main**, **Bias**, **PDE ADC TEMP**, **FEPD Settings**, and **AMUX**. Only **Main** is used.
Register History	④	Displays and clears the history of register writes and reads.
GUI Status Bar	⑤	Displays the GUI status and program errors.

- The details are covered in the PE1283X0/PE188X00 Up-Down Converter and Beamformer Evaluation Kit User's Manual.

Mixer Control GUI – Evaluation Software for PE128300



mmW GUI Main	Figure Ref.	Description
SPI HW Connection	①	Connects to SPI master device, displays the status of SPI connection, selects the SPI clock speed, initializes the PE128300, resets the SPI connection, and selects IF band to operate.
TCPIP Connection	②	Allows custom MATLAB scripts to utilize the tools in mmW GUI for automation, calibration, etc.
Register IO	③	Writes/reads one byte of data to/from selected device(s) and register address
Mixer Control	④	Selects one of the 32 pre-defined modes.
Debugging Tools	⑤	Not used (N/A).
Register History	⑥	Displays and clears the history of register writes and reads.

- The details are covered in the PE1283X0/PE188X00 Up-Down Converter and Beamformer Evaluation Kit User's Manual.

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