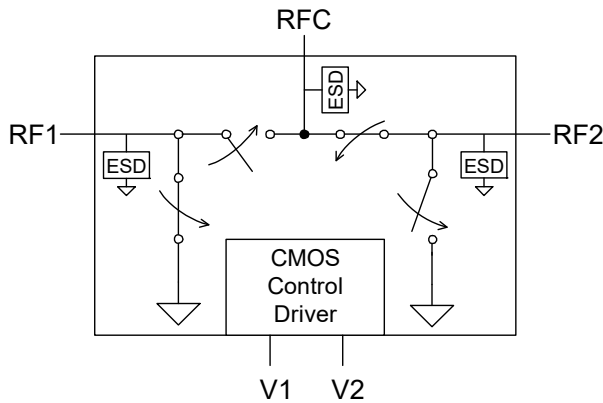


Product Description

The PE4250 is a HaRP™-enhanced reflective single-pole, double-throw (SPDT) RF switch for use in general switching applications and mobile infrastructure. This device offers a flexible supply voltage of 3.3V or 5V, single-pin or complementary pin control inputs, and 4000V ESD tolerance. It presents a simple alternative solution to pin diode and mechanical relay switches.

The pSemi HaRP™ technology enhancements deliver high linearity and exceptional performance. It is an innovative feature of the UltraCMOS® process.

Figure 1. Functional Diagram



SPDT UltraCMOS® RF Switch 10 MHz – 3 GHz, Reflective

Features

- HaRP-technology enhanced
- Low insertion loss: 0.65 dB @ 1000 MHz
- High isolation: 51 dB @ 1000 MHz
- P1dB typical: +30.5 dBm
- IIP3 typical: +59 dBm
- Fast switching time: 150 ns
- Flexible supply voltage: 3.3V ±10% or 5.0V ±10% supply (see Table 3)
- Excellent ESD protection: 4000V HBM
- No blocking capacitors required
- Single-pin or complementary control inputs

**Figure 2. Package Type
8-lead MSOP**

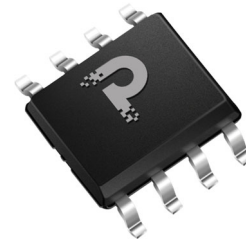


Table 1. Target Electrical Specifications, Temp = 25 °C, V_{DD} = 3.3 or 5.0V

Parameter	Conditions	Min	Typical	Max	Units
Operation frequency ¹	–	10	–	3000	MHz
Insertion loss (RF1/RF2)	10 MHz	–	0.6	0.65	dB
	1000 MHz	–	0.65	0.70	dB
	2000 MHz	–	0.75	0.80	dB
	3000 MHz	–	0.75	0.90	dB
Isolation (RFC to RF1/RF2)	1000 MHz	50	51	–	dB
	2000 MHz	46	48	–	dB
	3000 MHz	35	40	–	dB
Return loss	1000 MHz	–	25	–	dB
	2000 MHz	–	23	–	dB
	3000 MHz	–	20	–	dB
Input 1-dB compression ²	50–3000 MHz	–	30.5	–	dBm
Input IP3	50–3000 MHz, +18 dBm per tone, 5-MHz spacing	–	59	–	dBm
Switching time	50% CTRL to 10/90% RF	–	150	300	ns

Notes: 1. Device linearity can start to degrade below 10 MHz.

2. Absolute maximum rating of P_{IN} = 27 dBm.

Figure 3. Pin Configuration (Top View)

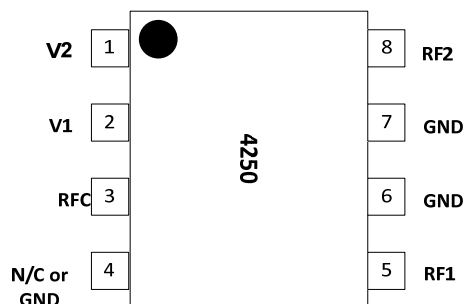


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V2	This pin supports two interface options: <ul style="list-style-type: none"> Single-pin control mode. A nominal 3.3V or 5V supply connection is required. Complementary-pin control mode. A complementary CMOS control signal to V1 is supplied to this pin.
2	V1	Switch control input, CMOS logic level
3	RFC	RF common port ¹
4	N/C or GND	No connect or ground
5	RF1 ¹	RF1 port ¹
6, 7	GND	Ground connections. For the best performance, ensure that the traces are physically short and connected to the ground plane.
8	RF2 ¹	RF2 port ¹

Note 1. All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V _{DD} power supply voltage ¹	3.0 4.5	3.3 5.0	3.6 5.5	V
I _{DD} power supply current V _{DD} = V _{CNTL} = 3.3V V _{DD} = V _{CNTL} = 5.0V	— —	55 75	60 80	μA
Control voltage high	0.8 x V _{DD}	—	—	V
Control voltage low	—	—	0.2 x V _{DD}	V
P _{IN} RF input power (50 Ω)	—	—	27	dBm
T _{OP} operating temperature range	-40	25	85	°C
T _{ST} storage temperature range	-65	25	150	°C

Note 1. Select either the 3.3 V or the 5.0 V power supply range.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	3	5.5	V
V _I	Voltage on any control input	-0.3	5.5	V
T _{ST}	Storage temperature range	-65	150	°C
P _{IN}	RF input power (50 Ω)	—	27	dBm
V _{ESD}	ESD voltage (HBM) ¹ ESD voltage (Machine Model)	—	4000 250	V

Note: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding the absolute maximum ratings could cause permanent damage. Restrict operation to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods can reduce reliability.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the specified rating.

Switching Frequency

The PE4250 has a maximum 25-kHz switching rate.

Moisture Sensitivity Level

The moisture sensitivity level (MSL) rating for the PE4250 in the 8-lead MSOP package is MSL3.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V2) = V _{DD} Pin 2 (V1) = High	RFC to RF1
Pin 1 (V2) = V _{DD} Pin 2 (V1) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 1 (V2) = Low Pin 2 (V1) = High	RFC to RF1
Pin 1 (V2) = High Pin 2 (V1) = Low	RFC to RF2

Control Logic Input

The PE4250 is a versatile RF switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- **Single-pin control mode:** The switch operates with a single control pin (pin 2) supporting a +3.3V or 5.0V CMOS logic input, and requires a dedicated +3.3V or 5.0V power supply connection (pin 1). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- **Complementary-pin control mode:** The switch operates using complementary control pins V1 and V2 (pins 2 and 1), that can be directly driven by +3.3V or 5.0V CMOS logic or a suitable microprocessor I/O port. This enables the PE4250 to operate in positive control voltage mode within its operating limits.

Evaluation Kit

The SPDT switch evaluation kit board was designed to ease customer evaluation of the PE4250 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the bottom SMA connector, J3. Port 1 and Port 2 are connected through 50 Ω transmission lines to two SMA connectors on either side of the board, J4 and J2. A through transmission line connects SMA connectors J5 and J6. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal-layer FR4 material with a total thickness of 0.0322." The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.033," trace gaps of 0.010," dielectric thickness of 0.028," copper thickness of 0.0021," and ϵ_r of 4.3.

J1 provides a means for controlling the DC inputs to the device. The second-to-bottom lower right pin (J1-3) is connected to the device V1 input. The second-to-top upper right pin (J1-7) is connected to the device V2 input. Footprints for decoupling capacitors are provided on both the V1 and V2 traces. The customer must determine the proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 4. Evaluation Board Layouts

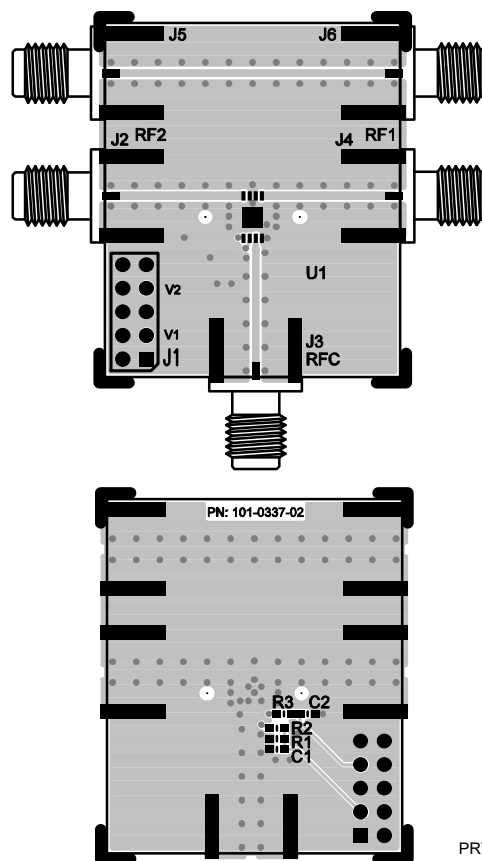
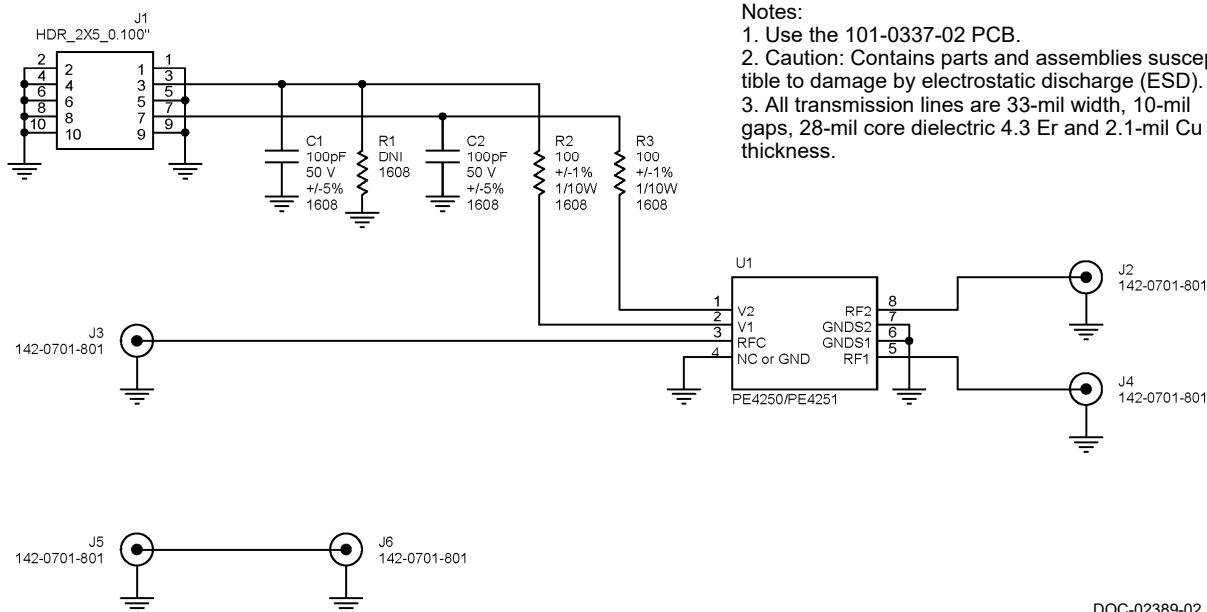


Figure 5. Evaluation Board Schematic



Typical Performance Data

Figure 6. Insertion Loss: RFC-RF @ 25 °C

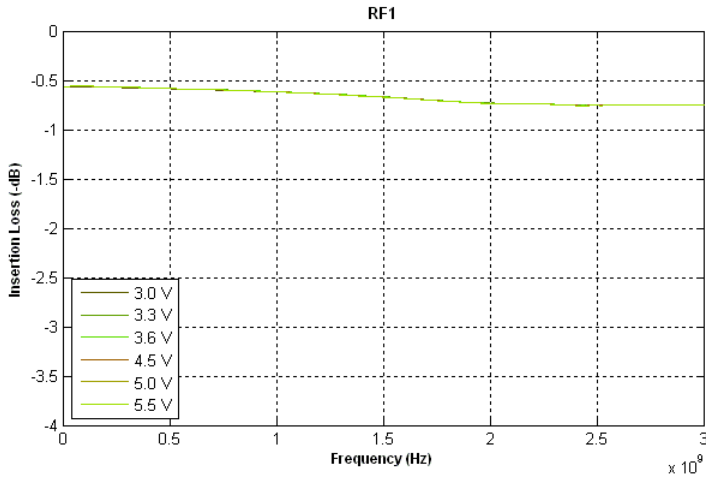


Figure 7. Insertion Loss: RFC-RF @ 3.3V

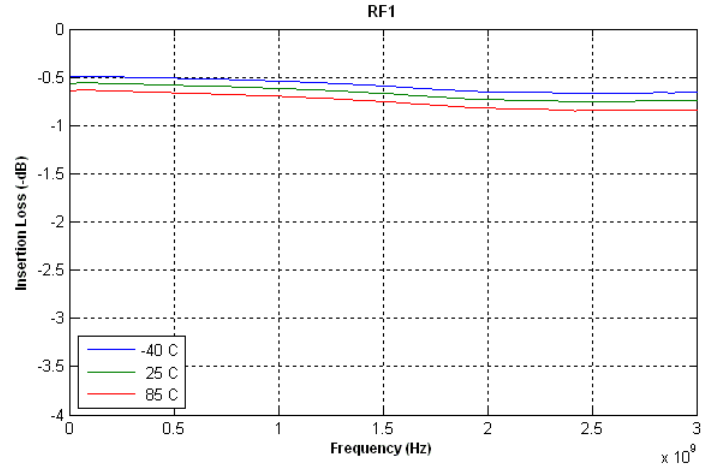


Figure 8. Isolation: RFC-RF @ 25 °C

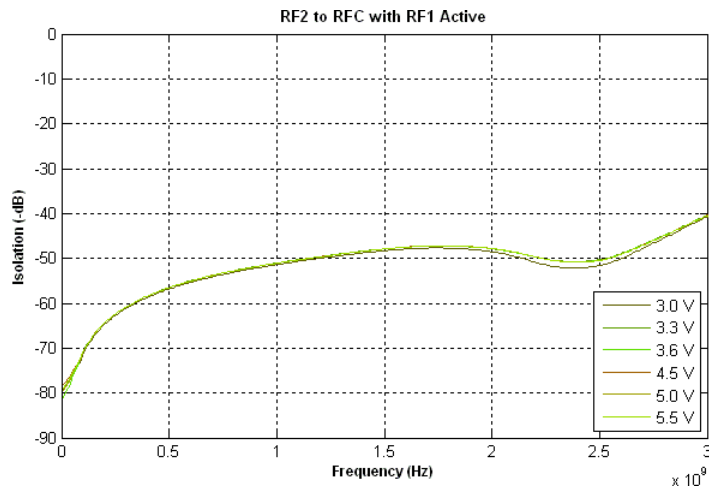


Figure 9. Isolation: RFC-RF @ 3.3V

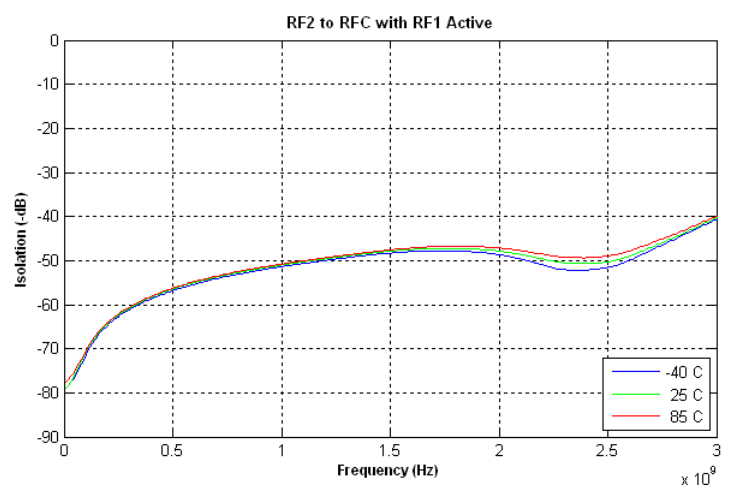


Figure 10. Return Loss at Active Port @ 25 °C

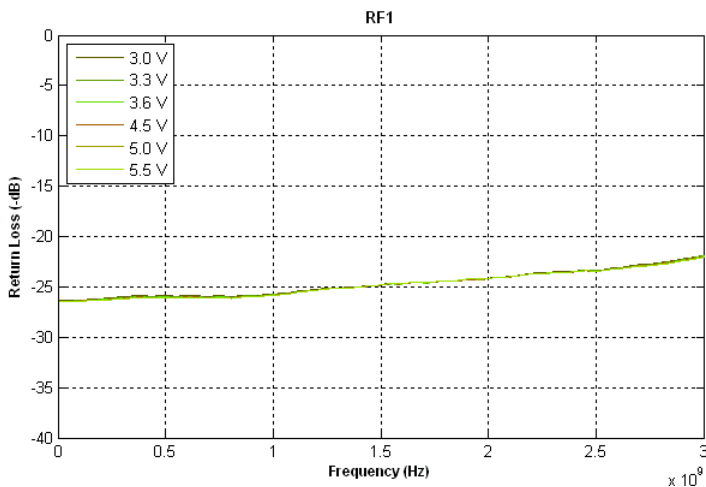


Figure 11. Return Loss at Active Port @ 3.3V

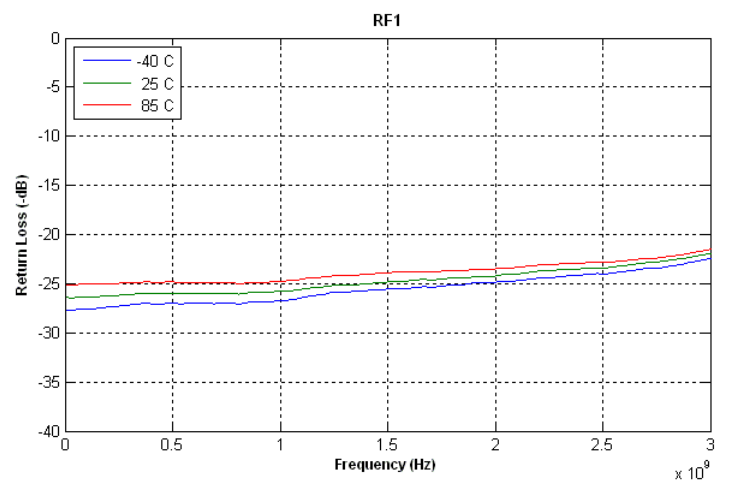


Figure 12. Package Drawing

8-lead MSOP: 19-0118-01

Notes: 1. Controlling dimension: inches.
2. Package length does not include mold flash, protrusions, or gate burr.
3. Package width does not include interlead flash or protrusions.

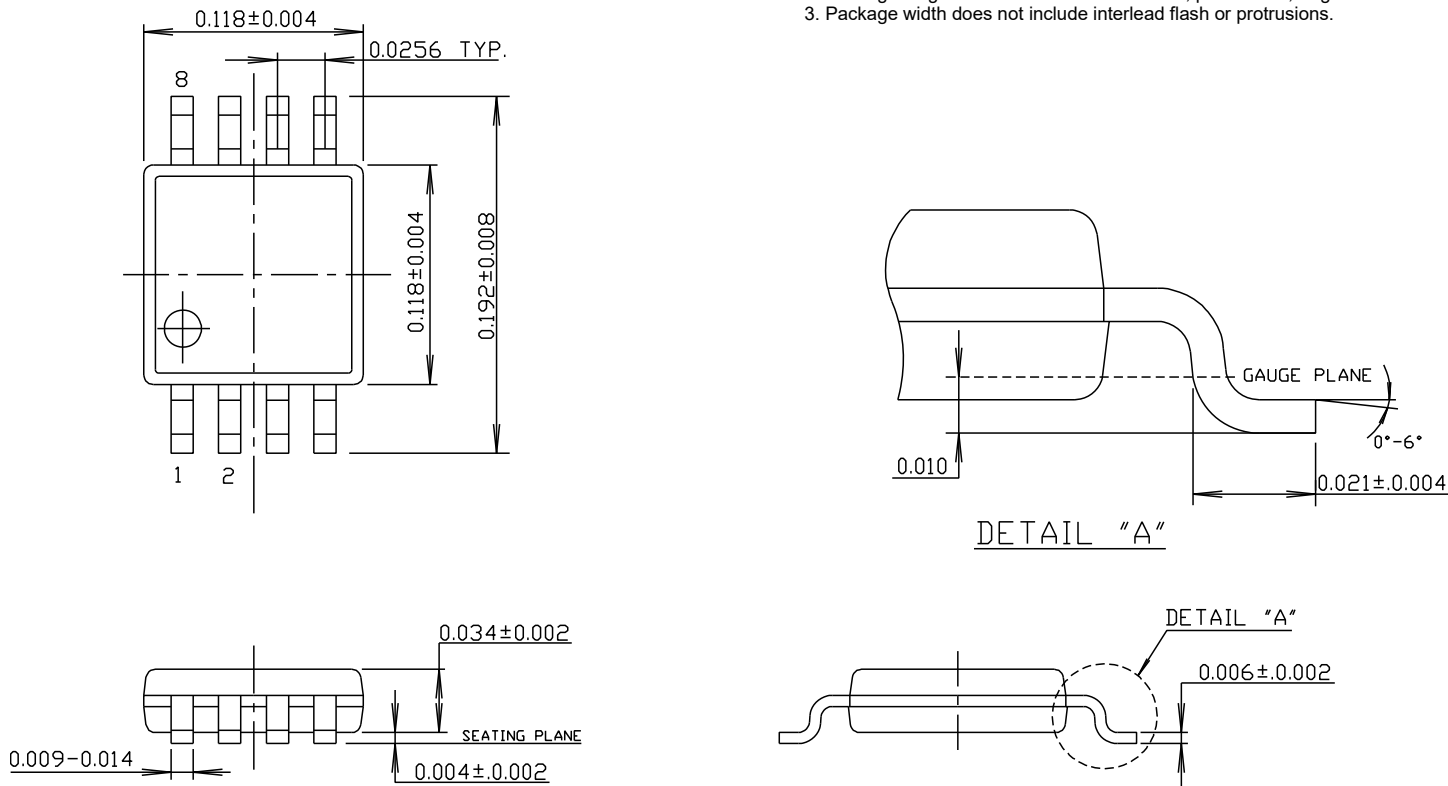
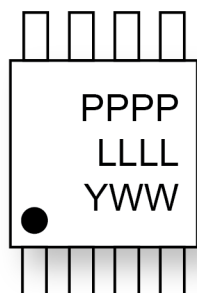


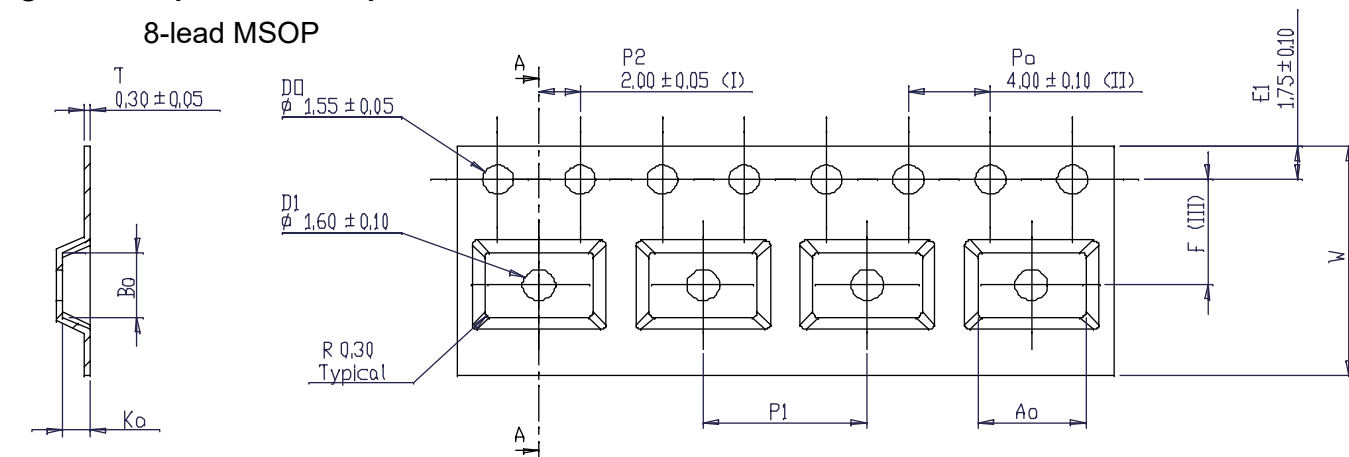
Figure 13. Top Marking Specification



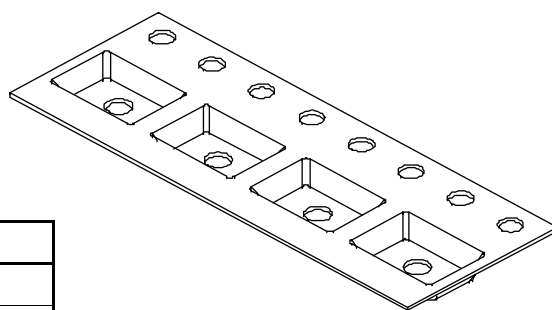
● = Pin 1 indicator
 P P P P = Product part number (4250 for PE4250)
 L L L L = Last four digits of the assembly lot number
 Y W W = Date code, last digit of the year, and work week

Figure 14. Tape and Reel Specifications

8-lead MSOP



SECTION A-A
SCALE 3.5 : 1

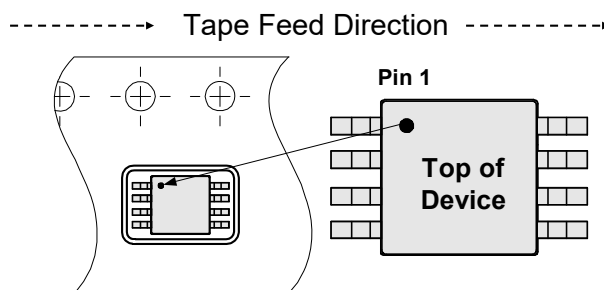


- (I) Measured from centreline of sprocket hole to centreline of packet,
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 ,
- (III) Measured from centreline of sprocket hole to centreline of packet,
- (IV) Other material available,

Table 7. Dimensions

Dimension	MSOP-8
Ao	5.30 ± 0.1
Bo	3.40 ± 0.1
Ko	1.40 ± 0.1
F	5.50 ± 0.05
P1	8 ± 0.1
W	12 ± 0.3

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED



Device Orientation in Tape

Table 8. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
EK4250-01	PE4250-EK	PE4250-08MSOP-EK	Evaluation kit	1/box
PE4250MLI	4250	PE4250G-08MSOP-cut tape or loose	Green 8-lead MSOP	Cut tape or loose
PE4250MLI-Z	4250	PE4250G-08MSOP-2000C	Green 8-lead MSOP	2000 units/tape and reel

Sales and Contact Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com.