

## PE826C32

## **Product Description**

The PE826C32 is a high performance monolithic CMOS RS-422 line receiver. Its operating supply range is 3.0 to 3.6V, with an input signal common mode range of +/-10V. The PE826C32 offers higher speed and lower power than other RS-422 receiver types. It is packaged in standard DIP and flat pack options and is ideal for stringent military applications.

The PE826C32 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the low power, economy and integration of conventional CMOS.

# Quad RS-422 Differential Line Receiver

#### **Features**

- High-speed operation: < 15 nS typical
- Low power: < 9 mA typical
- 3.3 V operation
- Standard packaging: 16-lead DIP and flat pack
- Pin Compatible with Existing Industry Products

Figure 1. Package Drawing

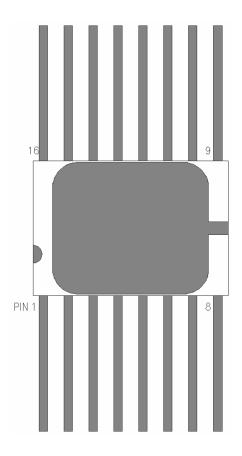
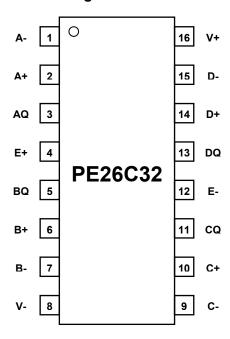


Figure 2. Pin Configuration



**Table 1. Pin Descriptions** 

Pin No.	Pin Name	Description	
1	A-	Channel A Inverting Input	
2	A+	Channel A Noninverting Input	
3	AQ	Channel A Output	
4	E+	Enable, active high	
5	BQ	Channel B Output	
6	B+	Channel B Noninverting Input	
7	B-	Channel B Inverting Input	
8	V-	Ground Pin	
9	C-	Channel C Inverting Input	
10	C+	Channel C Noninverting Input	
11	CQ	Channel C Ouput	
12	E-	Enable, active low	
13	DQ	Channel D Output	
14	D+	Channel D Noninverting Input	
15	D-	Channel D Inverting Input	
16	V+	Supply Pin	

**Table 2. Recommended Operating Conditions** 

Symbol	Parameter/Conditions	Min	Max	Units
V+	Supply voltage	3.0	3.6	V
T <sub>OP</sub>	Operating temperature range	-55	125	°C
VIN (Line)	Maximum input voltage A+/-, B+/-, C+/-, D+/-	-7	7	V
VIN (Dig)	Maximum input voltage	0	(V+)	V
VOUT	Maximum output voltage	0	(V+)	V
IOUT	Maximum output current	-10	10	mA
V <sub>ESD</sub>	ESD Voltage Human Body Model (Note 1)		1000	V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883 M3015 C2.

## **Electrostatic Discharge (ESD) Precautions**

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 2.

#### Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

#### **Device Functional Considerations**

The PE826C32 operates at high switching speeds. In order to obtain maximum performance, it is crucial that pin 16 be supplied with a bypass capacitor to ground (pin 8).

Table 3. Truth Table

E+	E-	Vin (Diff)	Q
L	Н	Х	Z
Н	Х	<-200 mV	L
Х	L		
Н	Х	>+200 mV	Н
Х	L		
Н	Х	Open	Н
Χ	L		



## **Table 4. Electrical Specifications**

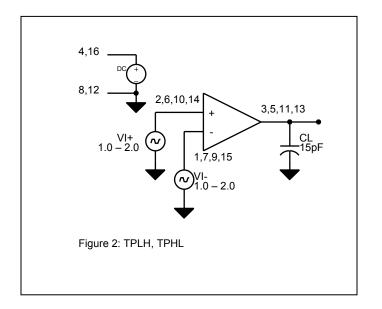
-55° C < Tcase < 125° C, 3.0 V < V+ < 3.6 V, PreRad, unless otherwise specified

Parameter	Minimum	Typical	Maximum	Units
Supply Voltage	3.0	3.3	3.6	V
Supply Current (Line inputs open, enabled) (V+)=3.6V		5	10	mA
Input Threshold (Line, differential) VCM=+7 VCM=0 VCM=-7	-200 -200 -200		200 200 200	mV mV mV
Input Threshold Hysteresis (Line, Differential) VCM=0	5	15	100	mV
Input Resistance (Line pins) VCM=+7 VCM=0 VCM=-7	15 K 15 K 15 K		25 K 25 K 25 K	Ohms Ohms Ohms
Input Current (Line pins) VCM=+7 VCM=-7	-1200		1000	uA
Input Threshold (Enable)	(V+)*0.3	(V+)/2	(V+)*0.7	V
Input Current (Enable)	-1		1	uA
Input "Failsafe" Open Circuit Differential voltage	200		2500	mV
Output Drive Current @ 0.5 V from rail (high or low)	10			mA
Output Short Circuit Current (to V-)	15		75	mA
Output Tristate Current, 0 < Vout < V+	-5		5	uA
VOH @ 10 mA	(V+) - 0.5 V	(V+) - 0.4	(V+)	V
VOL @ 10 mA	0	0.4	0.5 V	V
TPHL (See Fig 2)		12	25	nS
TPLH (See Fig 2)		12	25	nS
TPZL, TPZH (See Fig 3)		10	25	nS
TPHZ, TPLZ (See Fig 3)		10	25	nS
FMAX	50			MHz

Notes:

- (1) "Line" pins refer to A-, A+, B-, B+, C-, C+, D-, D+, differential outputs
  (2) "Digital Input" or "Enable" pins refer to E+, E(3) "Digital Input" pins refer to AQ, BQ, CQ, DQ
  (4) Output Short Circuit not intended to imply continuous operation

Figure 3. TPLH, TPHL Test Circuit Block Diagram



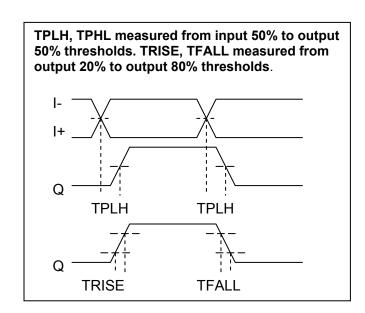
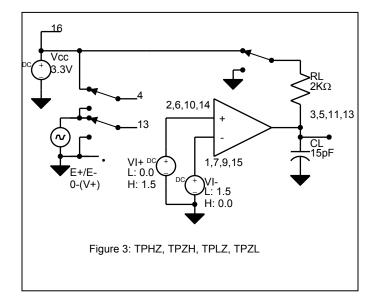
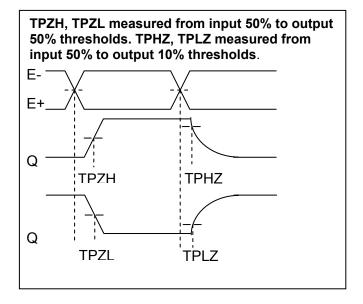


Figure 4. TPLZ, TPZL, TPHZ, TPZH Test Circuit Block Diagram







## **Table 5. Ordering Information**

Order Code	Part Marking	Description	Package	Shipping Method
<u>8</u> 26 <u>C</u> 32-01	PE826C32-01	Engineering Sample	16-pin DIP	1/Box
<u>8</u> 26 <u>C</u> 32-11	PE826C32-11	Production Unit, DIP	16-pin DIP	25/Tray
<u>8</u> 26 <u>C</u> 32-21	PE826C32-21	Production Unit, FP	16-lead FLAT PACK	25/Tray
<u>8</u> 26 <u>C</u> 32-00	PE826C32-EK	Eval <u>uation</u> Kit	Evaluation Board	1/Box



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## **Data Sheet Identification**

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The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

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### **Product Specification**

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